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Full-Wave Analysis of Power Distribution Networks in Printed Circuit Boards

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SUMMARY This paper provides an investigation of power distribution network (PDN) performance by a full-wave prediction tool and by experimental measurements. A set of six real boards characterized by increasing complexity is considered in order to establish a solid base for behaviour understanding of printed circuit boards. How the growing complexity impacts on the board performance is investigated by measurements and by simulations. Strengths and weakness of PDN modeling by the full-wave software tool Microwave Studio are highlighted and discussed.

key words: *decoupling capacitor, integrated circuits (ICs), power distribution network (PDN), printed circuit board (PCB), radiated and conducted emission, SPICE circuit simulator*

1. Introduction

The performance required by modern microcontrollers in automotive applications is becoming more and more demanding in terms of integration, execution speed and reliability. The IEC61967 standard [1] recommends to perform radiated emission test using a test board, sized to fit the TEM cell aperture, and exposing the device under test (DUT) to the detector structure inside the cell. The use of a suitable board is of major importance to minimize its contribution to the measured emissions. For this reason, great attention must be addressed to the design of the power distribution network (PDN). A proper understanding and characterization of PDN are very important to avoid or at least clearly identify emission peaks due to resonances on the PCBs and/or coming from discontinuities in the impedance profile versus frequency. The confidence acquired in the board performance allows one to better focus on real DUT emissions, screening out from the debugging process the parasitic contribution of the test environment. The main purpose of the board-level PDN is to distribute stable power from the voltage module regulator (VMR) to the electronics. However, switching circuitry demands static and dynamic current, which across the PDN impedance Z_{PDN} causes the voltage to fluctuate at the chip's power-supply terminals [2]. The noise circulating into power and ground planes can affect the operation of other active devices (signal/power integrity), as well as producing radiation (EMI). In order to effectively deliver power to the chip with minimal noise while reducing radiated emissions, the PDN input impedance Z_{PDN} needs to be as low as possible in the frequency range of interest, from DC to several hundreds of MHz. The use of decoupling capacitors allows to lower Z_{PDN} below a few hundreds of MHz [3], [4]. Above this frequency, their action as capacitance is affected by the parasitic inductance associated to the component itself and by the inductance associated to the component leads. In this task, simple and reliable simulation tools for the prediction of PDN resonances and of filtering performance by decoupling capacitors offer an attractive option, allowing board investigation before spending money and time in actual building a prototype. A further nice advantage is the possibility to probe the impedance at every location of the PCB, an operation that is practically impossible to do on the real board because of the probing constraints posed by instrumentation such as a network analyser. In the literature there are three main approaches used for the analysis of PDN. The first approach is based on the cavity mode model [5], [6] and allows very fast prediction of resonances for boards with simple structure. In case of complex structures the cavity model is combined to the segmentation method and its implementation requires experienced engineers. The second approach is based on PDN modeling by a SPICE circuit [7], [8]. This modeling is very convenient allowing simple, accurate and fast simulations, but it is difficult to use with complex boards having many planes and cuts. The third approach is based on the full-wave analysis by numerical methods [9]–[11]. These methods allow detailed modeling of complex configurations, but are very expensive in terms of computing time and memory requirements. The goal of this paper is to establish a solid base for PCB behaviour understanding through the investigation of six test boards which have been designed and manufactured at EURO Instruments. The test boards implement a PDN of growing complexity, from a simple pair of supply/ground planes with some decoupling capacitors, to a more complex structure with supply island, cuts in the planes, and multiple layers. The boards are modelled by the full-wave software tool MicroWave Studio (MWS), and the critical aspects to

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assure analysis effectiveness and accuracy are discussed.

2. Z_{PDN} versus Scattering Parameters

The analytical relation between Z and S parameters can be found in [12]. In practical cases, except possibly at parallel resonance frequency, the approximate relation:

$$Z_{\mathrm{PDN}} \approx 25\, S_{21} \tag{1}$$

can be used, since Z_{PDN} is much lower than the nominal characteristic impedance of the measurement system (i.e., $Z_0 = 50\,\mathrm{Ohm}$). This equation is valid with an error less of 1% up to the frequencies near the first series resonant frequency of the PCB caused by the inductance associated with the connection of the test ports and the board capacitance [2], [4]. Ideally, in point1 of a PCB where the IC switches, S_{11} should be maximized in order to have a very low Z_{11} (i.e., Z_{PDN}) in the frequency range of interest. On the contrary, S_{21} between point1 and point2 where another IC is placed, should be minimized in order to have strong attenuation of the Delta-I noise generated at point1 and propagating along the PCB. Owing to the approximate expression (1), and the perfect correspondence of resonant frequencies, in the following the results will be shown in terms of scattering parameters which are directly measured by a network analyzer and calculated in a straightforward way. For brevity, the results of the S_{21} parameter only are shown and commented. In any case, the discussion can be considered exhaustive since the two scattering parameters are characterized by the same resonant points.

3. Test Board Description

Six different test boards with increasing complexity are considered in order to allow a better understanding of the board behavior, and to highlight the scattering parameters change. For all six PCBs, the board dimensions are 10 cm × 10 cm, the distance between two nearby layers is 0.12 mm, and the dielectric substrate has relative permittivity $\epsilon_r = 4.3$ and loss tangent $\tan\delta = 0.02$. Some miniature coaxial connectors (SMA) are assembled on each test board in the same position to properly connect the network analyzer (NA) and allow reliable measurements. The six boards have in the same position, vias and cuts to allocate seven decoupling capacitors (indicated in the following as decaps for brevity). The nominal values of the decoupling capacitors are shown in Table 1. The description of the boards is as follows (see Figs. 1, 2) [15]:

- Board 1 has two layers: a top solid ground plane (see Fig. 1(a)), and a bottom solid power plane (as in Fig. 2(a), without the cut, the split)
- Board 2 has two layers: a top solid ground plane (see Fig. 1(a)), a bottom solid power and ground planes separated by a split (as in Fig. 2(a) without the cut)
- Board 3 is similar to Board 2, with a cut in the power plane (see Figs. 1(a) and 2(a)).

Table 1 Equivalent circuit parameters of decoupling capacitors.

	C	ESL	ESR
C1	33 nF	1.94 nH	0.297 Ω
C2	33 nF	1.94 nH	0.297 Ω
C3	100 nF	1.99 nH	0.128 Ω
C4	100 nF	1.99 nH	0.128 Ω
C5	100 nF	1.99 nH	0.128 Ω
C6	100 μF	2.5 nH	0.066 Ω
C7	100 μF	2.5 nH	0.066 Ω

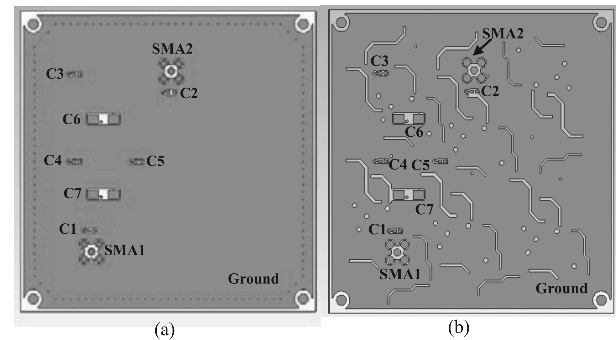


Fig. 1 Top view (ground plane) of Boards 1–5 (a), and of Board 6 (b).

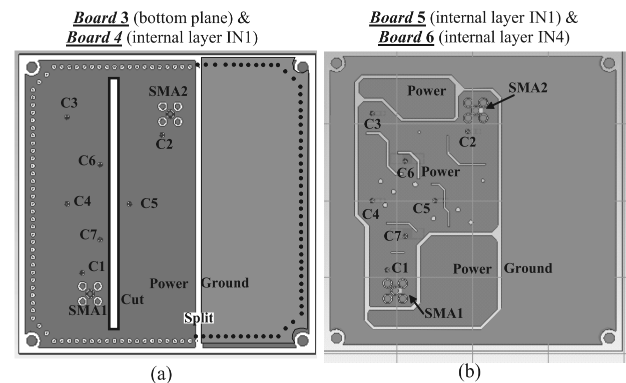


Fig. 2 Power plane view of Boards 3 and 4 (a), and 5 and 6 (b).

- Board 4 has three layers: a top and bottom solid ground planes as Fig. 1(a), and an internal IN1 solid power plane with a cut and ground plane as in Fig. 2(a).
- Board 5 has three layers: a top and bottom solid ground planes as in Fig. 1(a), an internal layer IN1 which has three islands of power (partitioning), and a ground that surrounds the power islands as in Fig. 2(b).
- Board 6 has six layers: the fourth internal layer IN4 has the same configuration of the internal layer of Board 5 (see Fig. 2(b)), while the top and bottom layers as well as the internal layers IN1, IN2 and IN3 are dedicated to ground. Top and IN1 layers have some discontinuities simulating holes and routings (see Fig. 1(b)).

The top ground plane of Boards 1–5 is shown in Fig. 1(a), while that of Board 6 is shown in Fig. 1(b). The power plane view of boards 3 and 6 is shown in Fig. 2. Note that even in Board 1 that is the simplest among those considered, there are several vias and cuts for SMA connectors and placement

of decoupling capacitors. The usage of three layer boards is acceptable for investigation purposes even if never applied in practice due to low mechanical performance.

4. Experimental Measurements

An experimental investigation on the six test boards has been performed at STMicroelectronics laboratory in Cornaredo (Italy). The experimental setup is shown in Fig. 3 where a board isolated from the ground is connected to the network analyzer. The scattering parameters were measured by an Agilent E8358 network analyzer, in the frequency range 300 kHz–2 GHz and adopting 1601 points. Two port SOLT calibration were initially performed using a Hewlett Packard 85052D calibration kit. The coaxial cables used between the network analyzer and the PCB under tests equipped with SMA connectors were the armoured workhorsetype with the following characteristics: 50 Ω characteristic impedance and −100 dB minimum relative shielding.

The S_{21} parameter has been measured for the six test boards without the presence of decoupling capacitors. The measurements of Fig. 4 show how S_{21} changes as the complexity of the PCB increases. Note that for all the considered boards the same reference points 1 an 2 were adopted, being the SMA connectors located in the same position. The results for S_{21} are compared using as a reference line −20 dB on the graphs and the following comments can be drawn:

- Board 1 has four points of resonance due to the fact that the two parallel planes behave like a resonant cavity.
- Board 2 has higher S_{21} at frequencies over 1 GHz than Board 1 due to the fact that the area of the power plane is reduced and the ground plane is extended in the same layer of the power and separated by a narrow split (partitioning effect).
- Boards 3 and 4 have the same S_{21} with points of resonance shifted towards lower frequencies compared with Board 2. This is due to the fact that board 3 has the same partitioning effect of Board 2 with in addition a long cut between point 1 and 2.
- Board 4 is similar to Boards 3 with an additional ground plane that does not change significantly S parameter curve.
- Board 5 is characterized by a first point of resonance shifted towards higher frequencies and higher values of S_{21} up to 2 GHz. This is due to the fact that the PCB is similar as Board 4 with the difference that partitioning effect is more complex and the area of power where the points 1 and 2 are placed is reduced.
- Board 6 has S_{21} values similar to Board 5 with a first point of resonance shifted towards higher frequencies. This is a 6-layers PCB similar to real PCBs with complex partitioning and several short cuts simulating component placements and routing.

Filtering of decoupling capacitors was also investigated. The S_{21} parameter in the absence and with decaps are shown in Fig. 5 in case of Boards 1, 3, and 6. The comparison shows that decoupling capacitors are ineffective in lowering S_{21} parameter over 150 MHz, owing to the inductive effect associated to the capacitors. A new resonance peak is introduced at 200 MHz by the capacitors. This is a parallel resonance due to the parasitic inductance of decaps that resonates with the PCB capacitance. Over 250 MHz the S_{21} parameters presents resonant points which depend on the structure of the PCB only, and not on decoupling capacitors that behave as a high inductive impedance. In conclusion, this investigation has shown:

- How resonance frequencies change depending on the number of layers and type of discontinuity such as vias, split, power islands, and short cuts.
- That the values of the S_{21} increases at higher frequen-

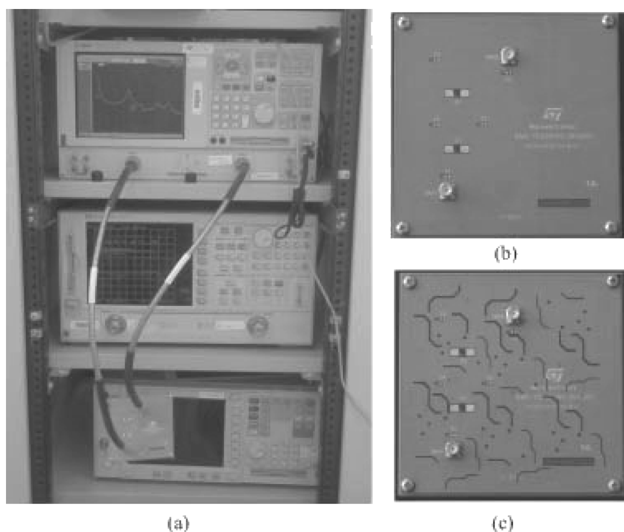


Fig. 3 Experimental activity at STMicroelectronics (Cornaredo, Italy): measurement setup (a), Board 3 (b) and Board 6 (c).

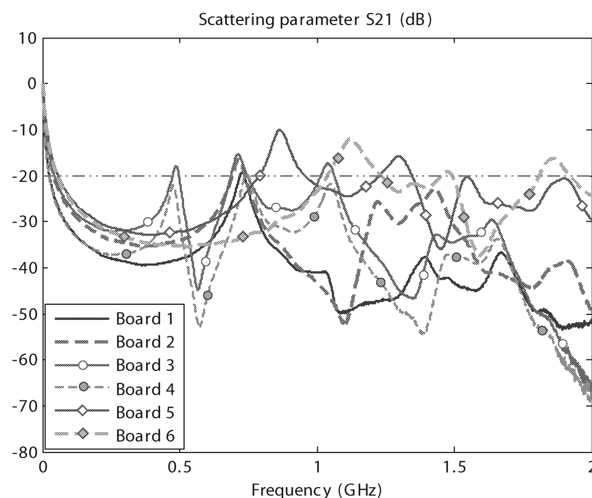


Fig. 4 Measured S_{21} for the six test boards considered in the absence of decoupling capacitors.

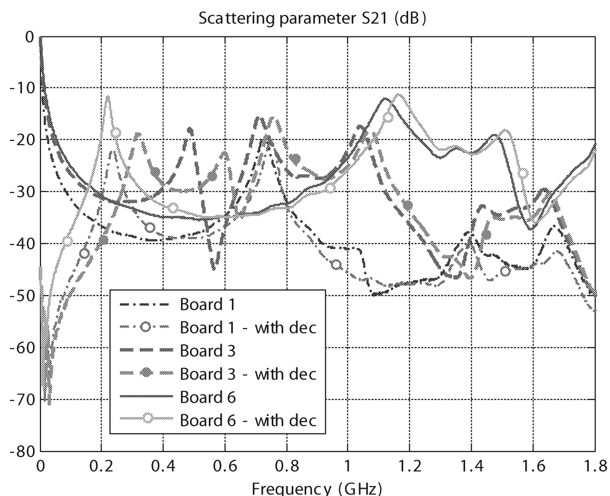


Fig. 5 Measured S_{21} for Boards 1, 3 and 6 in the absence and with decoupling capacitors.

cies as the board complexity.

5. PDN Investigation by a Full-Wave Software Tool

Full-wave numerical simulations were carried out by the software tool MicroWave Studio (MWS) based on the finite integration technique. This software has the great advantage of allowing the importation of the board configuration directly from CAD. It is known that full-wave simulation tools are suitable to provide a detailed analysis of complex structures, but they can require significant computational resources in terms of memory requirements and computing time. In order to achieve good results while keeping the computational requirements reasonable, the following crucial choices were made in setting up the simulation:

- The board layouts were imported by Gerber from the mechanical drawing of the board considering all the discontinuities such as vias, holes, and cuts for SMA connectors and for mounting decoupling capacitors.
- Power and ground planes were modeled as perfect electric conductors, i.e., no electric field tangential component ($E_t = 0$).
- The board side planes were modeled as perfect magnetic conductors, i.e., no magnetic field tangential component $H_t = 0$). This choice is reasonable when the analysis investigates the resonance frequencies of the board, and allows a strong reduction of the computational domain.
- The board excitation through SMA connectors was modeled by using a discrete port of length $l = 0.94$ mm placed in the ground plane as shown in Fig. 6(a). For a more accurate modeling of the board excitation, the SMA connector should be taken into account into the model, leading to a bigger computational domain and longer simulation time. In any case, as will be shown later by comparing the simulations with measurements, the approximation introduced will provide a good accuracy.
- Decoupling capacitors were modeled by lumped circuit elements having the nominal values of in Table 1. The lumped element length of capacitors C1-C5 was 0.6 mm, while that of capacitors C6-C7 was 3.18 mm.

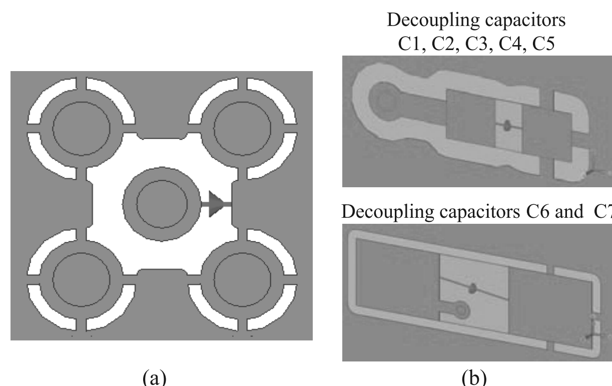
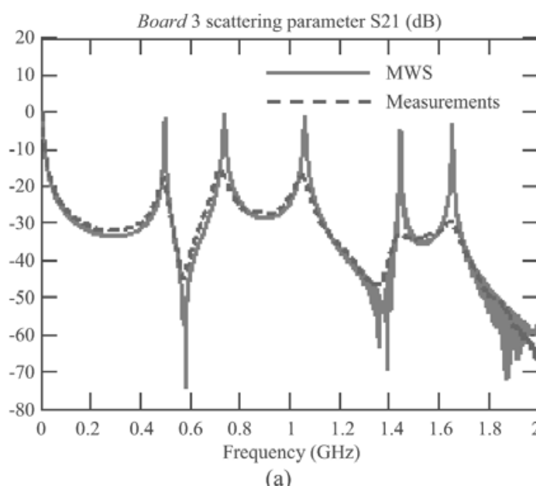


Fig. 6 MWS modeling of SMA connectors by a discrete port (a) and of decoupling capacitors by lumped elements (b).



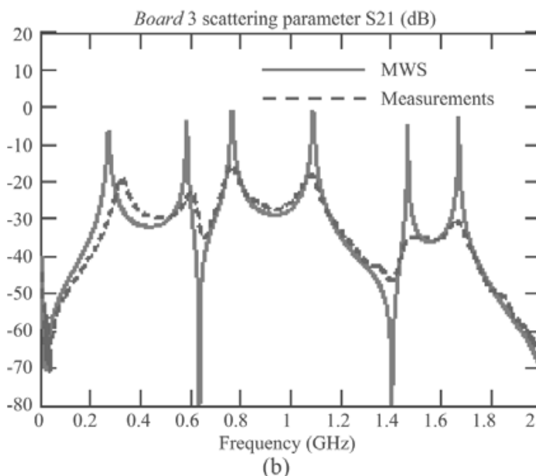


Fig. 7 Scattering parameter S_{21} in case of Board 3: without (a) and with (b) decaps.

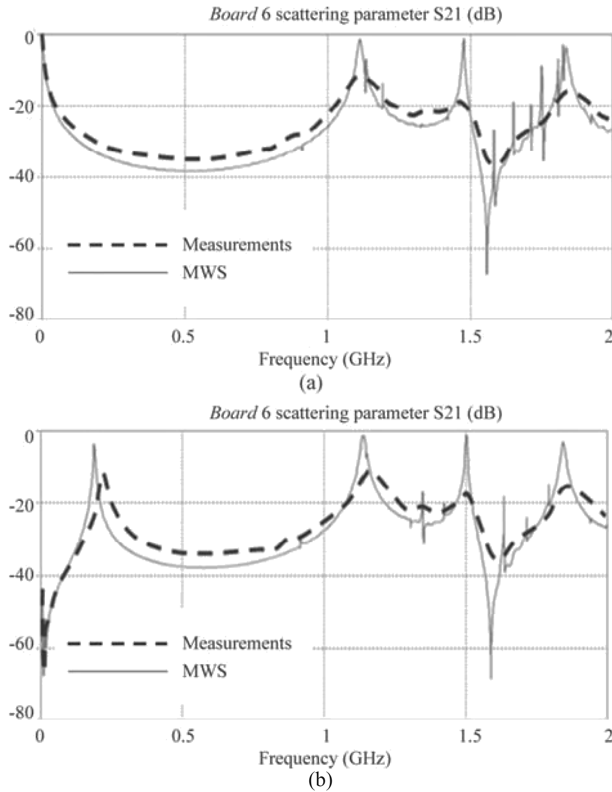


Fig. 8 Scattering parameter S_{21} in case of Board 6: without (a) and with (b) decaps.

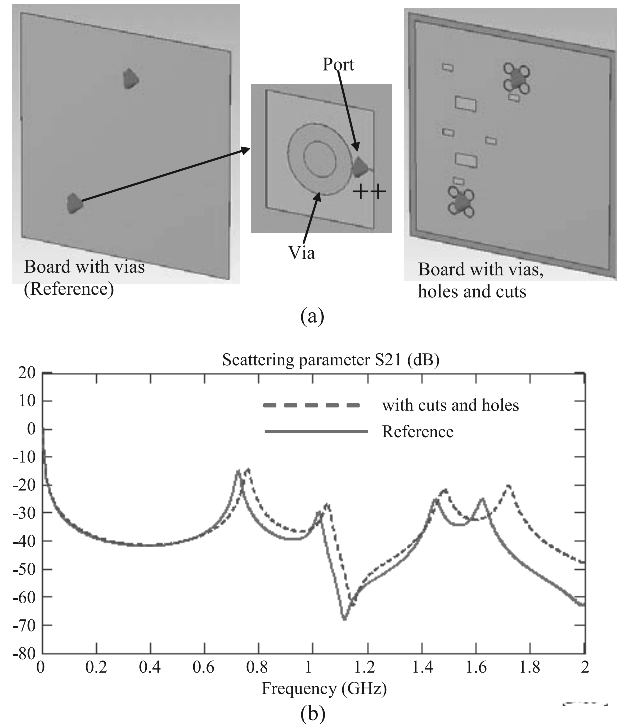


Fig. 9 MWS model of the simplified Board 1 without and with cuts and holes (a), and calculated scattering parameter S_{21} (b).

Results of MWS simulations obtained in the cases of Boards 3 and 6 without and with decaps are shown in Figs. 7, 8. Measurements and numerical simulations for both Boards 3 and 6 are in good agreement, apart from the sharper resonance peaks computed by MWS and a slight shift of the first resonance when decaps are present. The sharper peaks obtained by MWS are due to the fact that losses were neglected in the simulations in order to speed up the calculation. The reduction of this first resonance frequency computed by MWS is due to the extra inductance associated to the finite dimension of the lumped elements used to model the capacitors. Note that especially in case of C6 and C7, this inductance is not negligible, it is on the order of 2 nH as can be seen by applying (4), and assuming $r_{\text{via}} = 0.1$ mm. In case of Board 6 there are also some discrepancies above 1.5 GHz due to some spikes present in the numerical solutions. Simulations also confirm that decoupling capacitors are effective in lowering S_{21} up to 150 MHz. An additional resonance peak appears at 200 MHz due to the inductive effect of the capacitors. Moreover, above 300 MHz the S_{21} parameter is not affected by capacitors. To verify the impact of real test board cuts, holes, vias, and decoupling capacitor pads, an additional investigation was performed by MWS simulations. Two configurations of simplified Board 1 wihout and with vias, cuts, and holes are modeled (see Fig. 9(a)). The comparison of simulation results is shown in Fig. 9(b) and it clearly highlights the S_{21} increase due to the presence of vias, cuts and holes. This section has shown that the full-wave simulation can reproduce the measurements with very good accuracy even in the case of complex multilayer boards. The main drawback of this approach is the long computational time required, and it doesn't allow fast investigation of physical phenomena causing EMI. For this purpose, it is convenient to use other approaches such as the cavity model [2], [4] which is very suitable for modeling parallel solid planes with and without decoupling capacitors, or SPICE circuit modeling that allows a fast investigation of EMI phenomena involved [2].

6. Low-Frequency SPICE Model for Decoupling Capacitor Investigation

When the interest is focused on the effects of decoupling capacitors only, a low-frequency (LF) SPICE circuit can be used as a very simple, convenient, and fast prediction tool [4]. However, the LF circuit model does not account for PCB resonances due to the cavity effect. The main parameters considered by this model are:

1. The intrinsic capacitance C_{PCB} between the two planes (i.e., inter-plane capacitance).
2. The inductance L_S associated to the source.
3. The equivalent series R, L, C circuit of the decoupling capacitors.

A critical issue in setting up this circuit is the calculation of the source inductance L_S that can be expressed as

$$L_S = L_{\text{board}} + L_{\text{via}} \tag{2}$$

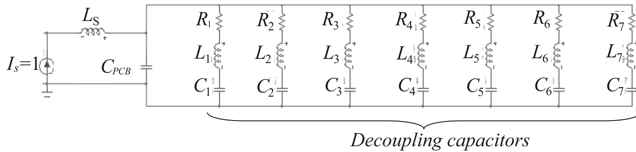


Fig. 10 LF-circuit model of Board 1 with decoupling capacitors having the nominal values of parasitic parameters as reported in Table 1.

where L_{board} is the radial inductance of the board seen from the connection points of the source to the PCB, and L_{via} is the via inductance. Under the assumption that the field perturbation due to the switching device travels outwards from the component with cylindrical symmetry, the generated waves move as in a radial transmission line which behaves as a non-uniform TL with line inductance and capacitance depending on the radial distance r from the origin [2], [13], [14]. In that case, the board radial inductance L_{board} can be calculated by the radial transmission line theory as:

$$L_{\text{board}} = \int_{r_{\text{via}}}^{r_2} \mu d/(2\pi r) dr \tag{3}$$

where r_{via} is the source via radius, and r_2 defines the board maximum extension. Note that since the radial inductance decreases inversely as the distance from the source, it is reasonable to neglect the inductance at distances greater than twenty times rvia and assume $r_2 = 20 r_{\text{via}}$ in (3). The via inductance can be derived by the application of the partial inductance concept as:

$$L_{\text{via}} = \frac{\mu_0}{2\pi} d \left(\ln\left(2d/r_{\text{via}}\right) - 1\right) \tag{4}$$

where d is the substrate thickness. This expression is valid for $r_{\text{via}} \ll d$ [2]. When r_{via} is comparable with d, a more complicated expression should be used [2]. In the case of Board 1, L_{via} is negligible compared to L_{board}, as d very small, and $L_S = 0.072$ nH is obtained. Note that this approach based on the radial TL theory allows a fast approximate estimation and an easy physical interpretation of the L_S parameter. A more accurate prediction of L_S can be derived by the cavity mode method as described in [15]. By this approach, in the case of Board 1 $L_S = 0.095$ nH is obtained. The LF circuit model of Board 1 is shown in Fig. 10 where $L_S = 0.095$ nH, $C_{\text{PCB}} = 3.173$ nF, and the RLC circuits of decaps have the nominal values shown in Table 1. The PDN impedance calculated by the LF circuit in case of simplified Board 1 and Board 1 with decaps are shown in Fig. 11, and the results are compared with those obtained by the more accurate high-frequency circuit model described in [2]. Note that the first dip in case of simplified board (see Fig. 11(a)) is due to the inductance associated to the source. A filtered board would have no resonance points if decaps were not affected by parasitic inductance as shown by the dotted line in Fig. 11(b). In this case, even the first series resonance due to the source inductance disappears due to the fact that C_{PCB} is much lower than decaps capacitance. It can be also observed that the resonant frequencies exhibited by Z_{PDN} in Fig. 11 coincides with those of scattering parameter

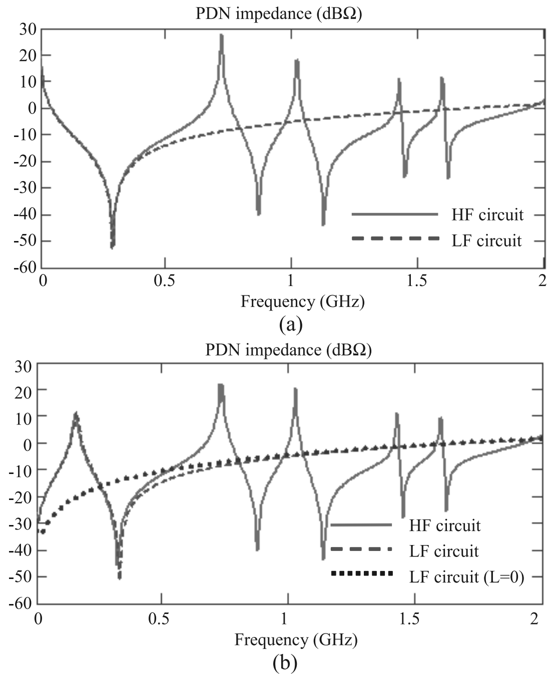


Fig. 11 Comparison S_{21} calculated by the HF- and by the LF-circuit models: bare board 1 (a) and board 1 with decaps (b).

S_{21} shown in Fig. 9. The LF circuit model is very simple to form and allows fast prediction, but it can compute the first resonant frequency only.

7. Conclusions

Boards of increasing complexity have been investigated by experimental measurements and by a full-wave prediction tool. The investigation has highlighted that:

- Z_{PDN} is the main parameter to show the ability of the fixes adopted (i.e., decoupling capacitors, embedded capacitance, etc.) in mitigating EMI phenomena in a PCB such as delta-I noise and emissions.
- Numerical tools are suitable to reproduce S parameters obtained by measurements, and therefore Z_{PDN} also, for complex boards with several planes where vias, short cuts and power islands are present.
- A correct interpretation of numerical simulations and measurements can be done if the associated inductance to the sourcing port and the nearby discontinuities for SMA connector are taken into account.
- The effectiveness of decoupling capacitors is limited to the low frequency range (i.e., below 500 MHz).
- The use of a full-wave analysis is required to predict resonant frequencies of complex boards with vias, cuts, splits, multiple planes.

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