PAPER

A Pulse-Tail-Feedback LC-VCO with 700 Hz Flicker Noise Corner and −195 dBc FoM

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SUMMARY This paper proposes a pulse-tail-feedback VCO, in which the tail transistor is driven using pulse-shaped voltage signals with rail-to-rail swing. The proposed pulse-tail-feedback (PTFB) VCO relies on reducing the current conduction period of the tail transistor and operating the tail transistors in triode region for reducing the flicker and thermal noise from the active elements. Mathematical analysis and circuit level simulations of the phase noise mechanism in the proposed PTFB-VCO is also presented in this paper for validating the effectiveness of the proposed technique. A prototype LC-VCO with the proposed PTFB technique is fabricated in a standard 180 nm CMOS. Laboratory measurement shows a power consumption of 1.35 mW from a 1.2 V supply at 4.6 GHz. The proposed PTFB-VCO achieves a flicker corner of 700 Hz, which enables the VCO to maintain a fairly constant figure-of-merit (FoM) of −195 dB within a wide offset frequency range of 1 kHz–10 MHz.

key words: *oscillator, LC-VCO, PLL, flicker noise, pulse VCO, phase noise, tail feedback*

1. Introduction

Wireless communication has advanced tremendously in the past decades. Over the generations, wireless communication speed has undergone a steady growth and with the rolling out of the fifth generation wireless (5G) standard, the data rate capability of the mobile devices will have improved by thousands of folds as compared to the earlier generations. The advancements in CMOS manufacturing technology enables the low-cost fabrication of digital baseband systems that can support multi-Gpbs data rate. Unfortunately, advanced technology nodes does little to improve the performance of RF front end modules, especially the local oscillator (LO). In fact, the process scaling typically has a negative impact on the LO performance. Hence it is necessary to develop new design techniques that can address the factors degrading the LO performance at a more fundamental level.

Phase Locked Loops (PLL) are widely used as LOs in most of the modern wireless transceivers. For ensuring better modulated signal quality (EVM), it is important to reduce the jitter (or phase noise) [1]–[4] generated by the PLL. In a typical analog PLL as shown in Fig. 1, one of the most critical sources of jitter is the Voltage Controlled Oscillator (VCO) [3], [4]. Figure of Merit (FoM) is an excellent tool for evaluating the performance of various VCO circuits since it enables fare comparison between different topologies. It must be noted that the FoM that is being referred to in this paper [5] normalizes the phase noise at a given offset with the oscillation frequency and power consumption as given by the following equation:

$$FoM = \mathcal{L}(\Delta\omega) - 20\log\left(\frac{\omega}{\Delta\omega}\right) + 10\log\left(\frac{P_{\mathrm{DC}}}{1\,\mathrm{mW}}\right) \quad (1)$$

where $\mathcal{L}(\Delta\omega)$ is the phase noise at an offset of $(\Delta\omega)$ from the carrier *omega*, and P_{DC} is the power consumption. The importance of the VCO is only magnified since it is also one of the most power-hungry components in a typical PLL. Increasing power can improve the VCO jitter [6]. However, this is not a viable option in the modern wireless era.

A quick review of the VCO phase noise reveals that it is composed of the white $(1/f^2)$ noise, which appears in the phase noise plot with a slope of −20 dB/dec., and the up-converted flicker noise $(1/f^3)$, which exhibits a slope of −30 dB/dec. as shown in Fig. 2 (a). The point of inter-

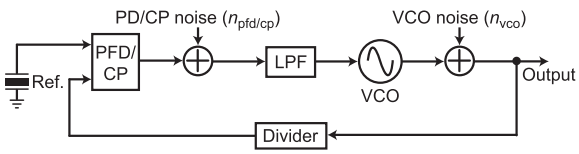

Fig. 1 Simplified PLL phase noise model showing major noise sources.

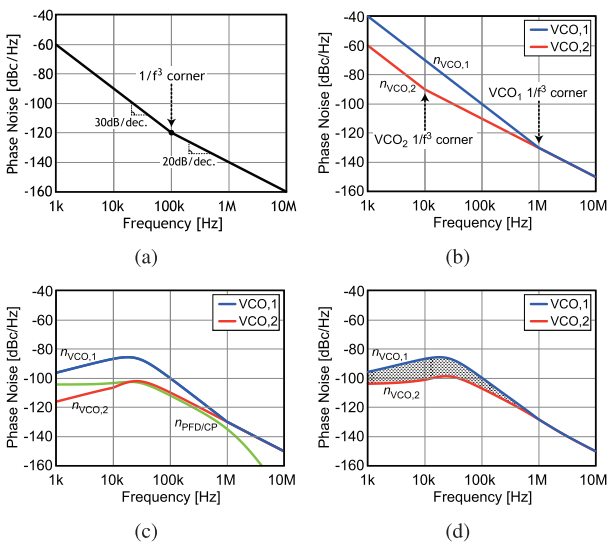

Fig. 2 Effect of VCO flicker noise on PLL jitter (a) phase noise characteristics of a typical VCO (b) open loop phase noise plots of two VCOs with 1 kHz and 1 MHz flicker noise corner (c) closed loop noise transfer function for PLL components (VCO_1, VCO_2 and PFD/CP) (d) overall jitter of the PLL while using VCOs with different flicker corner.

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section of these two curves is known as the flicker corner ($1/f^3$). The formulation of the theory of Impulse Sensitivity Function (ISF) [7], [8] enhanced our understanding of phase noise in oscillators and enabled researchers to develop techniques for designing power-efficient low-noise oscillators [9], [10]. However, most of the conventional VCO architectures focus on reducing the noise contribution from the white noise component [9]–[21] and these techniques are typically ineffective in dealing with the flicker noise. This work presents an alternative approach for reducing the jitter contribution of the VCO by reducing the both the white noise and flicker noise components. Examining Fig. 2 (b) to Fig. 2 (d), it can be seen that a VCO with low flicker noise can be used for reducing PLL jitter.

Conventional techniques used for reducing VCO flicker noise are based either on filtering out the noise [22], [23] or on minimizing Groszkowski effect [24]–[26]. Noise filtering techniques introduces significant area overhead due to the additional LC tank, and the Groszkowski effect minimization typically requires transformers [26] or resistors [25] along with the LC tank, which could result in $1/f^2$ noise degradation. A tail-feedback technique has been proposed for LC-VCOs [27]–[29] for improving the current-efficiency and $1/f^3$ noise corner of LC-VCO by limiting the current conduction time (conduction angle) of the tail transistor. In this method, it is necessary to keep the tail transistors saturated for lowering the conduction angle. The flicker corner reduction capability of this technique is limited to hundreds of kilohertz [27]–[29]. A modified tail-feedback VCO architecture using PMOS type tail current source proposed in [30] hypothesized that noise filtering can be achieved by driving the tail transistors into deep triode region. Even though this technique can reduce the flicker corner well below tens of kilohertz, the analysis done in this paper reveals that it suffers from a trade-offs between $1/f^3$ corner, $1/f^2$ noise, and power efficiency. This ultimately lowers the figure-of-merit (FoM) at high offset frequencies with lowering flicker corner. Since the tail-feedback VCO does not require additional inductor, they have the added advantage of being area efficient. However, as explained above, the conventional implementations of tail-feedback VCOs suffer from a clear trade-off between flicker noise corner and $1/f^2$ noise. This paper analyzes the phase noise mechanism in conventional tail-feedback VCOs [27]–[30] in detail, and proposes a new technique namely "pulse-tail-feedback" (PTFB) [31], which has the capability to lower the flicker noise corner without compromising the VCO FoM. This paper also presents one possible circuit implementation of the proposed pulse-tail-feedback VCO in standard 180 nm CMOS process.

2. Flicker Reduction Using Pulse-Tail-Feedback Technique

2.1 Conventional Tail-Feedback VCO

The tail-feedback LC-VCO has been developed for improving the current efficiency and for reducing the flicker noise [27]–[30], which has its roots in the pioneering work done by various researchers [32]–[36] on the effects of switched biasing on flicker noise. Tail-feedback technique exploits the time-variant nature of the VCO for periodically switching the tail transistor through "on" and "off" states. This reduces the flicker noise generated by the tail transis-

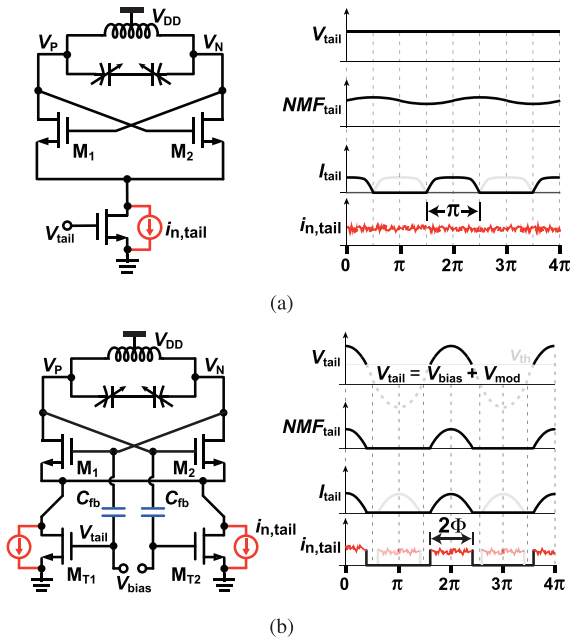


Fig. 3 Current-biased VCOs depicting their schematics (left) and conceptual waveforms showing noise injection (right) for (a) constant tail-bias and (b) modulated tail-bias using tail-feedback [27]–[29].

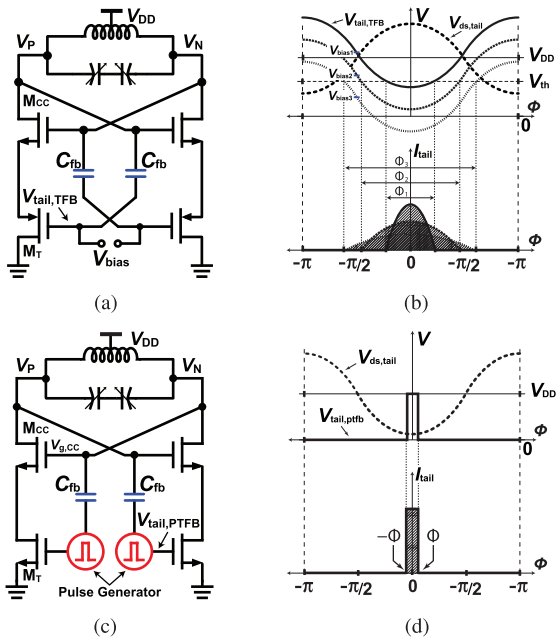


Fig. 4 Simplified circuit schematic of (a) the modified tail-feedback VCO [30] and (c) the proposed pulse-tail-feedback VCO [31] along with (b), (d) their corresponding voltage and current waveforms.

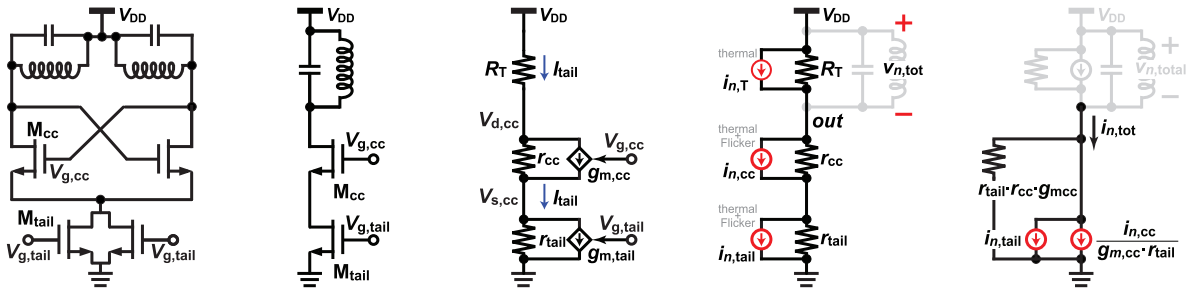


Fig. 5 (a) Simplified circuit schematic for a differential current-biased LC-VCO (b) single branch of the VCO (c) simplified small signal model (d) major sources of noise (e) simplified noise model.

tor by reducing the memory effect of the trapped carriers in the gate oxide [32]–[36]. A typical constant current-biased VCO is shown in Fig. 3 (a). Recalling that the noise injected into the tank is the product of the noise generated by the tail transistor and the noise multiplying function at the tail node (NMF_{tail}) [7], it can be concluded that the noise from the tail transistor is injected into the tank for the entire period of oscillation in a VCO with constant tail-bias. In a conventional tail-feedback VCO such as the one shown in Fig. 3 (b) [27]–[29], the fundamental oscillations coupled through the capacitors (C_{fb}) are combined with a DC bias (V_{bias}) as the driving signal for the tail transistors M_{T1} and M_{T2}. It can be noted from Fig. 3 (b) that by lowering the DC bias (V_{bias}), the overdrive voltage of the tail transistors (V_{OD}) can also be lowered, which controls the conduction period of the transistors. One half of the conduction period is termed as the conduction angle (Φ) and it can be expressed as:

$$\cos(\Phi) = \frac{V_{\text{OD}}}{A_{\text{T}}} = \frac{V_{\text{th}} - V_{\text{bias}}}{A_{\text{T}}} \tag{2}$$

where A_{T} is the amplitude of tank oscillations. By reducing the conduction angle, the amount of noise injected into the tank can also be reduced. However, in order to reduce conduction angle in conventional tail-feedback VCOs, it is necessary to maintain very low overdrive voltage for the tail transistors as evident from Figs. 4 (a) and (b).

2.2 Pulse-Tail-Feedback VCO

The proposed pulse-tail-feedback VCO achieves conduction angle reduction by using pulses for driving the tail transistors. Since the conduction angle is controlled only by the width of the pulses, there is no restriction on the overdrive voltage applied to the tail transistors, as in the case of conventional tail-feedback VCO. It can be observed from Fig. 4 (c) and (d) that the conduction angle reduction is be achieved by using pulse-shaped signals with controllable pulse widths for driving the tail transistors. The advantage of using pulse signals for conduction angle reduction is that, unlike the conventional TFB technique, the proposed PTFB technique does not require a reduction in the transistor overdrive voltage (V_{OD}) for lowering the conduction angle [31]. The dependence of the tail transistor overdrive voltage and the VCO phase noise is analyzed in detail in Sect. 2.3.

2.3 Phase Noise Mechanism in Current-Biased VCOs

A typical differential current-biased VCO with the LC-tank split between the two branches of the differential pair is shown in Fig. 5 (a). Owing to the time-variant nature of the VCO, the circuit can be simplified as shown in Fig. 5 (b). The main sources of phase noise are shown in Fig. 5 (c), which can be identified as; (i) the tank noise ($i_{\text{n,T}}$), (ii) noise from the cross coupled transistor ($i_{\text{n,cc}}$), and (iii) noise from the tail transistor ($i_{\text{n,tail}}$). Note that the tank noise source is purely thermal due to the resistive element R_{T}, whereas the noise from the active elements ($i_{\text{n,cc}}$ and $i_{\text{n,tail}}$) is composed of both thermal and flicker noise [37]. *i.e.*

$$\overline{i^2_{\text{n,tail}}} = 4k_{\text{B}}T\gamma \cdot gm_{\text{tail}} + \frac{K}{C_{\text{ox}}(WL)_{\text{tail}}}\frac{1}{f} \cdot gm^2_{\text{tail}} \tag{3}$$

$$\overline{i^2_{\text{n,cc}}} = 4k_{\text{B}}T\gamma \cdot gm_{\text{cc}} + \frac{K}{C_{\text{ox}}(WL)_{\text{cc}}}\frac{1}{f} \cdot gm^2_{\text{cc}} \tag{4}$$

$$\overline{i^2_{\text{n,T}}} = \underbrace{4k_{\text{B}}T \cdot R_{\text{T}}}_{\text{thermal}} \qquad \underbrace{\qquad\qquad}_{\text{flicker}} \tag{5}$$

where k_{B} is the Boltzmann's constant, T is the absolute temperature in degrees Kelvin, γ is the empirical constant for MOSFET, K is an empirical constant, f is the frequency offset, and gm_{cc} and gm_{tail} represents the transconductance of the cross-coupled transistor and tail transistor, respectively. Since the noise model of a MOSFET depends on its operating region [38], the expression for the transconductance (gm_{x}) presented here is modified to include the effects of MOSFET operating region (*i.e.* saturation/triode). From the phase noise expression ($\mathcal{L}(\Delta\omega)$) developed by A. Hajimiri and T.H. Lee [7], [8], the oscillator phase noise at an offset $\Delta\omega$ can be represented as:

$$\mathcal{L}(\Delta\omega) = 10\log\left[\frac{\sum_i N_{L,i}}{2\Delta\omega^2 C^2 A^2_{\text{tank,diff}}}\right] \tag{6}$$

where tank capacitance $C = Q/(\omega_{\circ}R)$, $A_{\text{tank,diff}}$ is the differential voltage across the tank network and $N_{L,i}$ is the effective noise generated by the i^{th} device and is defined as [9]:

$$N_{L,i}(t) = \frac{1}{T_0}\int_0^{T_0} \Gamma^2(t)\,\overline{i_{n,i}^2(\phi)}\,\mathrm{d}t \tag{7}$$

where $\Gamma^2(t)$ is the impulse sensitivity function (ISF) at the node under consideration [7]. This paper extends the analysis done in [9], [10] by including the effects of the tail-current source. It can be observed from Fig. 5 (d) that three main noise sources are present in a typical current biased VCO (i) tank noise ($N_{\mathrm{L,tank}}$ due to the noise current $i_{\mathrm{n,T}}$) (ii) noise from the tail transistors ($N_{\mathrm{L,tail}}$ due to the noise current $i_{\mathrm{n,tail}}$) and (iii) noise from the cross coupled transistors ($N_{\mathrm{L,cc}}$ due to the noise current $i_{\mathrm{n,cc}}$). Figure 5 (d) also reveals that the MOSFETs (cross coupled MOS and the tail MOS) along with the tank impedance forms a current divider network. As a result, only a fraction of the noise generated by the active elements (cross coupled MOS and the tail MOS) flows into the tank, which is rendered as the VCO phase noise. Since multiple uncorrelated noise sources are present, superposition theorem can be applied to quantify the effective noise current delivered to the tank network ($\overline{i_{\mathrm{n,tot}}^2}$) as:

$$\overline{i_{\mathrm{n,tot}}^2} = \overline{i_{\mathrm{n,T}}^2} + \overline{i_{\mathrm{n,tail}}^2} + \overline{i_{\mathrm{n,cc}}^2} \tag{8}$$

where $\overline{i_{\mathrm{n,T}}^2}$, $\overline{i_{\mathrm{n,tail}}^2}$, and $\overline{i_{\mathrm{n,cc}}^2}$ are the noise currents generated from the tank resistance (R_{T}), the tail MOSFET current (I_{tail}) and the cross coupled pair current (I_{cc}), respectively. A brief discussion on each of these noise sources is presented hereafter for intuitively understanding their influence on the phase noise in conventional TFB-VCO and proposed PTFB-VCO. The validity of this intuitive analysis will be corroborated using the mathematical analysis and circuit level simulations presented in Sect. 2.4.

The noise contribution from the tank impedance can be calculated as [9]:

$$N_{\mathrm{L,tank}} = \frac{1}{2\pi}\int_{-\pi}^{\pi}\left(4\mathrm{k_B T}\cdot\frac{1}{R_{\mathrm{T}}}\right)\mathrm{d}\phi \tag{9}$$

For accurate and fair comparison of the conventional TFB-VCO and the proposed PTFB-VCO, this paper makes use of the excess noise factor (ENF) [39], which normalizes the noise contributions from the active elements with the tank noise thus facilitating the deduction of the effects of tank noise ($N_{\mathrm{L,tank}}$) from the analysis. Following the analysis in [39], *ENF* of the i^{th} device working in a specified operating *region* can be defined as:

$$ENF_{i,region} = \frac{1+\frac{N_{\mathrm{L,i,region}}}{N_{\mathrm{L,tank}}}}{\eta_{\mathrm{P}}} \tag{10}$$

where $N_{\mathrm{L,i,region}}$ is the noise from the i^{th} device while working in the specified *region* of operation. and η_{P} represents the power efficiency, which is the product of voltage efficiency and current efficiency ($\eta_{\mathrm{V}} \times \eta_{\mathrm{I}}$).

The remaining elements contributing to the VCO phase noise are the tail transistors and the cross coupled transistors. It can be noticed from Fig. 5 (c) that the current in the tail transistor is composed of two components:

$$I_{\mathrm{tail}} = I_{\mathrm{r,tail}} + I_{\mathrm{gm,tail}} \tag{11}$$

$$= \frac{V_{\mathrm{s,cc}}}{r_{\mathrm{tail}}} + g_{\mathrm{m,tail}}V_{\mathrm{g,tail}} \tag{12}$$

where $I_{\mathrm{r,tail}}$ is the portion of tail current flowing through the resistive element of the tail MOSFET, and $I_{\mathrm{gm,tail}}$ is the portion of tail current flowing through the (trans)conductive element of the tail MOSFET, the noise generated by which can now be calculated as [9]:

$$i_{\mathrm{n,tail}}^2(\phi) = 4\mathrm{k_B T}\cdot\gamma g m_{\mathrm{tail}}(\phi) \tag{13}$$

where gm_{tail} is dependent on the operating region of the MOSFET [38], [40]. That is, for a MOSFET working in saturation condition, the main source of noise is the transconductance itself, which is also evident from Eq. (12) as $r_{\mathrm{tail}} \to \infty$ in saturation. In contrast, the noise current in a MOSFET working in triode region is dependent on the drain-to-source voltage (source voltage of the cross coupled transistor $V_{\mathrm{s,cc}}$ as shown in Fig. 5 (c)) as well. From Eqs. (12) and (13), it can be seen that driving the tail transistor into deep triode region forces most of the tail current to flow through the resistive element instead of the transconductive element, thus reducing the noise generation. From Eq. (11), there are two options for maintaining a specified I_{tail}: (i) increase gm_{tail}, (ii) decrease r_{tail}. The modified TFB-VCO using PMOS type tail current source as shown in Fig. 4 (a) [30] drives the tail transistors into deep triode region using large gate bias voltage which reduces r_{tail} and facilitates flicker noise reduction through filtering action. However, from Eq. (2) and Fig. 4 (a), large gate bias results in a large conduction angle which results in larger period of noise injection and lower current efficiency, which ultimately results in a lowering of FoM. On the other hand, the conventional TFB-VCO as shown in Fig. 3 (b) reduces the noise generation and noise injection by reducing the conduction angle (Φ), which is accomplished by using gate bias voltage that is well below the threshold voltage [27]–[29]. But from Eq. (2), maintaining small conduction angle requires lowering the overdrive voltage thus forcing the transistors to operate in saturation region. As a result, no noise filtering can be achieved at the tail node and almost all the noise generated by the tail transistor is injected directly into the tank and translated into the phase noise. In conclusion, in conventional TFB-VCO and modified TFB-VCO, the requirement for lowering the conduction angle (Φ) directly contradicts with the requirement for noise filtering, and as a result these VCOs are not capable of lowering noise generation and achieving noise filtering simultaneously.

The noise contribution of the cross coupled transistors to the VCO phase noise can be found by following the analysis done by A. Mazzanti and P. Andreani [9]. The main difference between the analysis done in this work as compared to [9] is that in Eq. (A5) of [9], it is assumed that the cross coupled transistor current is dependent only on the gate voltage. This is only true for transistors working in saturation region (which is the case for a class-C VCO [9]). However, for the proposed PTFB-VCO shown in Figs. 4 (c)

and (d), the cross coupled transistors enter deep-triode region within the conduction period of the tail transistors. *I.e.* if the conduction angle Φ of the tail transistors are small enough, within the conduction angle, the gate potential of M_{cc} ($V_{g,cc}$) traverses the voltage maxima while its drain potential (V_P or V_N) traverses the voltage minima.

Owing to the similarities of modified TFB-VCO in Fig. 4 (a) to the conventional TFB-VCO shown in Fig. 3 (b), the latter is selected for detailed analysis and comparison with the proposed PTFB-VCO [31] in this paper.

2.4 Comparison of Noise Generated in Conventional Tail-Feedback and Proposed Pulse-Tail-Feedback

From Fig. 5 (c), voltages at various nodes of the cross coupled transistor and tail transistor can be listed as:

$$V_{d,cc}(\phi) = V_{DD} - A_T \cos(\phi) \tag{14}$$

$$V_{g,cc}(\phi) = V_{DD} + A_T \cos(\phi) \tag{15}$$

$$V_{g,tail}(\phi) = V_{bias} + A_T \cos(\phi) \tag{16}$$

where $V_{d,cc}(\phi)$, $V_{g,cc}(\phi)$ and $V_{g,tail}(\phi)$ represents the voltages at the drain of the cross coupled transistor pair, gate of the cross coupled pair and gate of the tail transistor, respectively. V_{bias} is the DC bias applied to the tail transistor in conventional tail-feedback VCO, V_{DD} is the supply voltage, and A_T is the amplitude of tank oscillations across R_T due to the fundamental current ($I_{\omega_\circ}$), which is defined as:

$$A_T = I_{\omega_\circ} \cdot R_T \tag{17}$$

In a conventional TFB-VCO as the one shown in Fig. 3 (b), the cross coupled pair is working in class-B mode, it can be predicted with a fair amount of certainty that the cross coupled transistor turns "on" in triode region for the most of its conduction period. Also, from [27]–[29] and from the discussion in Sect. 2.3, it is clear that the tail transistor in a conventional TFB-VCO stays in saturation region while it conducts current. The currents flowing in cross coupled transistor and the tail transistor can be expressed respectively as:

$$I_{cc,tri}(\phi) = \beta_{cc,tri}(V_{gs,cc}(\phi) - V_{th} - V_{ds,cc}(\phi))V_{ds,cc}(\phi) \tag{18}$$

$$I_{tail,sat}(\phi) = \beta_{tail,sat}(V_{gs,tail}(\phi) - V_{th})^2 \tag{19}$$

where $V_{gs,cc}(\phi)$, $V_{ds,cc}(\phi)$, and $V_{gs,tail}(\phi)$ are the potential differences between gate-source terminal of cross coupled transistor, drain-source terminal of cross coupled transistor, and the gate-source terminal of tail transistor, respectively. The parameter β_x accounts for the physical parameters of the device, which can be represented as:

$$\beta_x = \frac{1}{2}\mu_n C_{ox}\left[\frac{W}{L}\right]_x \tag{20}$$

where μ_n is the mobility of electrons (μ_p for p-channel devices), C_{ox} is the oxide capacitance, $[W/L]_x$ is the width (W) to length (L) ratio of the x^{th} device. The DC component of the current flowing in the transistors is equal to the tail bias current (I_{tail}) over one oscillation cycle and it can be represented as:

$$I_\circ = \frac{1}{2\pi}\int_{-\Phi}^{\Phi} I_{tail}(\phi)\,d\phi \tag{21}$$

From [29], [31] and from Fig. 9 (b), it can be noted that the tail current (I_{tail}) in both conventional TFB-VCO and the proposed PTFB-VCO is set by the bias current (I_B), the size ratio between the bias transistor (M_B) and the mirroring tail transistor (M_T), and the conduction angle (Φ). Using Fourier's theory, the fundamental harmonic component of the current flowing in a transistor can be expressed as:

$$I_{\omega_\circ} = \frac{1}{\pi}\int_{-\Phi}^{\Phi} I(\phi)\cos(\phi)\,d\phi \tag{22}$$

The fundamental current in the tail transistor can be thus calculated as:

$$\begin{aligned} I_{\omega_\circ,tail} &= \frac{1}{\pi}\int_{-\Phi}^{\Phi} I_{tail}(\phi)\cos(\phi)\,d\phi \\ &= \frac{\beta_{tail}A_T^2}{6\pi}\Big[\Big(6\sin(\Phi) - 6\sin(\Phi)\cos(\Phi)^2\Big) \\ &\quad - \Big(6\Phi\cos(\Phi) + 3\sin(2\Phi)\cos(\Phi) + 2\sin(\Phi)^3\Big)\Big] \end{aligned} \tag{23}$$

Since the fundamental component of the current flowing in the cross coupled transistor is same as that of the tail transistor, it can be written that:

$$I_{\omega_{\circ,cc}} = I_{\omega_\circ,tail} \tag{24}$$

Assuming that β_{cc} is equivalent to β_{tail}, it can be deduced from Eq. (24) that:

$$\beta_{tail} = \frac{15\pi}{2A_T\Phi^5 R_T} \tag{25}$$

The solution for β_{tail} obtained above is back substituted for calculating power efficiency and transconductance. In a differential VCO, $I_{tail} = 2 \times I_\circ$. The DC to RF current conversion efficiency can be thus calculated as:

$$\eta_I = \frac{1}{\sqrt{2}} \cdot \frac{I_{\omega_\circ}}{2I_\circ} = \frac{1}{\sqrt{2}} \cdot \frac{I_{\omega_\circ}}{I_{tail}} \tag{26}$$

Assuming an ideal LC tank with an impedance of R_T at a frequency of $\omega_\circ$, the voltage at the output node V_P of a typical differential VCO can be written as:

$$V_P(\phi) \approx V_{DD} - \frac{R_T}{2} I_{\omega_\circ}\cos(\phi) \tag{27}$$

As $A_T = 1/2(\sqrt{2}R_T\eta_I I_{tail})$ from Eqs. (17) and (26), the differential output voltage of a VCO can be calculated as:

$$\begin{aligned} V_{out}(\phi) &= V_P(\phi) - V_N(\phi) = R_T I_{\omega_\circ}\cos(\phi) \\ &= -2A_T\cos(\phi) \end{aligned} \tag{28}$$

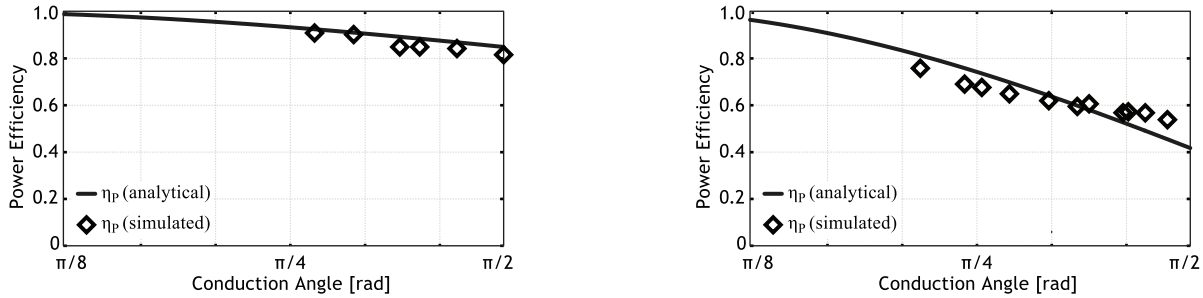


Fig. 6 Power efficiency of (a) TFB VCO and (b) PTFB VCO as a function of the conduction angle.

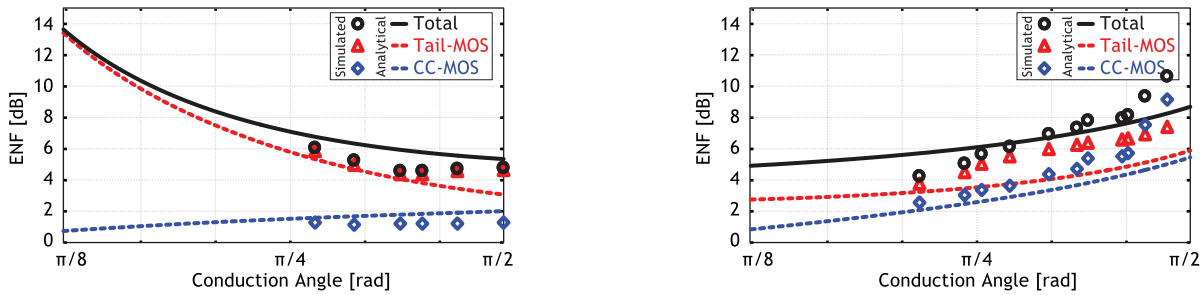


Fig. 7 Calculated ENF of (a) conventional TFB-VCO and (b) proposed PTFB-VCO as a function of the conduction angle.

Considering rms value of the tank voltage amplitude as $V_{\mathrm{RF,rms}}$, the voltage efficiency of a typical differential VCO is then calculated as:

$$\eta_{\mathrm{V}} = \frac{V_{\mathrm{RF,rms}}}{V_{\mathrm{DD}}} = \frac{\sqrt{2}A_{\mathrm{T}}}{V_{\mathrm{DD}}} \tag{29}$$

Assuming a voltage limited operation, the conventional TFB-VCO such as the one shown in Fig. 3 (b) achieves a maximum efficiency of $\sqrt{2}$. The power efficiency (η_{P}) is calculated as the product of η_{I} and η_{V}, and the results are plotted in Fig. 6 (a). Since the tail transistor in a conventional TFB-VCO operates in saturation region, its transconductance can be calculated as:

$$gm_{\mathrm{tail,sat}}(\phi) = \frac{\partial I_{\mathrm{ds}}(\phi)}{\partial V_{\mathrm{gs}}(\phi)} = \frac{2I_{\mathrm{tail,sat}}(\phi)}{V_{\mathrm{gs,tail}}(\phi) - V_{\mathrm{th}}} \tag{30}$$

Recalling from Eq. (3) that the noise power spectral density of a transistor that is generating a current of $i_{\mathrm{n},\omega_\circ}$ is proportional to the transconductance of the device [40], its thermal noise can be calculated as:

$$i^2_{\mathrm{n,tail,sat}}(\phi) = 4\mathrm{k_B T}\gamma gm_{\mathrm{tail,sat}}(\phi) \tag{31}$$

The noise contribution of the tail transistor can be now calculated using Eq. (7) as:

$$N_{\mathrm{L,tail,sat}}(\phi) = \frac{1}{2\pi}\int_{-\pi}^{\pi} \Gamma^2_{\mathrm{t}}(\mathrm{t})\overline{i^2_{\mathrm{n,tail,sat}}(\phi)}\,\mathrm{d}\phi$$
$$= \frac{5\mathrm{k_B T}\gamma \mathrm{h}^2}{2(\Phi)^5 R_{\mathrm{T}}} \times \Big(3\cos(\Phi)\sin(2\Phi) + 4\sin(\Phi)^3 - 12\sin(\Phi) + 6(\Phi)\cos(\Phi)\Big) \tag{32}$$

where $\Gamma^2_t(t)$ is the ISF at the tail node [7]. The noise contribution from the tail transistor in a conventional TFB-VCO can be now calculated using the ENF given by Eq. (10) as:

$$ENF_{tail,sat} = 1 - \frac{5\gamma}{4(\Phi)^5} \times \Big(3\cos(\Phi)\sin(2\Phi) + 4\sin(\Phi)^3 - 12\sin(\Phi) + 6(\Phi)\cos(\Phi)\Big) \tag{33}$$

Unlike the tail transistor, the cross coupled transistor pair in a conventional TFB-VCO enter triode region for most of its operating period. Keeping this in mind, the ENF of the cross coupled transistors is calculated following similar analysis as above. The resulting ENF of the tail transistor and the cross coupled transistor in a conventional TFB-VCO is plotted in Fig. 7 (a). As hypothesized in Sect. 2, the noise from the cross coupled pair decreases as the conduction angle reduces, whereas an increase in noise contribution from tail transistor can be observed with the lowering of conduction angle. From Eq. (8), the total noise from the active elements is calculated as the sum of their individual noise contributions, which is shown using solid black line in Fig. 7 (a).

Following the procedure followed for analyzing the conventional TFB-VCO noise as above, the noise analysis of the proposed pulse-tail-feedback VCO can be carried out. The main distinction of the proposed PTFB-VCO from the conventional TFB-VCO is that the tail-transistors in the proposed PTFB-VCO are operated in the triode region instead

of saturation region for reducing the noise generation as hypothesized in Sect. 2. This is made possible in the PTFB-VCO by facilitating the conduction angle (*Phi*) control via control of the pulse width of the signal that is fed back to the tail transistor. Thus, the proposed PTFB-VCO does not suffer from the interdependence between the transistor overdrive voltage, V_{OD} and the conduction angle, Φ (*i.e.* conduction angle can be reduced without having to reduce the transistor overdrive voltage as shown in Fig. 4 (d)) [31]. The cross coupled pair in the proposed PTFB-VCO functions like the cross coupled pair in conventional TFB-VCO since they work in class-B mode.

From the above discussion, we can conclude that the node voltages of the cross coupled transistors are similar to that of the conventional TFB-VCO and can be represented using Eqs. (14) and (15). The gate voltage of the tail transistor is assumed to be a pulse shaped voltage signal, which can be represented as:

$$V_{g,tail,ptfb}(\phi) = V_{DD} \tag{34}$$

The fundamental current flowing in the tail transistor of the proposed PTFB-VCO can be calculated using Eq. (22) as:

$$I_{\omega_\circ,ptfb} = 1 - \frac{\Phi^2}{6} + \cdots \tag{35}$$

The current efficiency of the proposed PTFB-VCO is calculated from Eqs. (26) and (35). While the voltage efficiency of the proposed PTFB-VCO follows Eq. (29) (since the cross coupled transistors work in class-B mode). Multiplying the current and voltage efficiency gives the power efficiency of the proposed PTFB-VCO, which is plotted in Fig. 6 (b). It can be observed from Fig. 6 that operating the tail transistors in triode region results in a lower current efficiency (and thus a lower power efficiency) at larger conduction angles as compared to operating the tail transistors in saturation. However, at smaller conduction angles, the gap between the power efficiency of the proposed PTFB-VCO approaches that of the conventional TFB-VCO. Recalling that in the proposed PTFB-VCO, the tail transistor turns on in triode region when it is conducting current, its transconductance ($gm_{tail,ptfb}(\phi)$) and noise ($N_{L,tail,sat}(\phi)$) can be calculated as:

$$gm_{tail,ptfb}(\phi) = \beta_{tail,ptfb} \cdot V_{ds,tail,ptfb}(\phi) \tag{36}$$

$$N_{L,tail,sat}(\phi) = \frac{k_B T \gamma h^2 \beta_{tail,ptfb} V_{ds,tail,ptfb}(\phi)}{3\pi} \times \left((3\sin(2\Phi) + 6\Phi)V_{DD} + 4A_T \sin(\Phi)^3 - 12A_T \sin(\Phi)\right) \tag{37}$$

From the above results and Eq. (10), the ENF of the tail transistor in the proposed PTFB-VCO is calculated and plotted in Fig. 7 (b).

Comparing the ENF of the conventional TFB-VCO and the proposed PTFB-VCO as shown in Fig. 7, the advantages of the proposed PTFB-VCO becomes evident. It can be noticed that as the conduction angle (Φ) is lowered below $\pi/2$, the ENF in the conventional TFB-VCO is worsened due to the increase in noise generation from the tail transistors. In stark contrast, a decrease in ENF is observed with lowering conduction angle in the proposed PTFB-VCO, thanks to the pulse-based tail biasing technique.

2.5 Simulations

Circuit level simulations were carried out on the conventional TFB-VCO, as depicted in Fig. 3 (b), and the proposed PTFB-VCO, as depicted in Fig. 4 (d), using Cadence Virtuoso (ADE L) environment to substantiate the validity of the analysis presented in Sect. 2.4. Real circuit models from the PDK of TSMC 180 nm process were used for the cross coupled transistors, the tail transistors and the tank elements. Verilog-A based models were used in place of the pulse generator of the proposed PTFB-VCO for better controllability of the pulse width of the fed back signal. The use of a Verilog-A based model also helps in understanding the circuit behavior in the presence of a delay in the pulse generator circuitry by facilitating variable delay addition (details of this will be presented in Sect. 3.2). Power efficiency of the conventional TFB-VCO and the proposed PTFB-VCO were simulated using harmonic balance (hb) simulations and the results are superimposed on the analytical results shown in Fig. 6. Phase noise analysis is done using periodic steady state (pss) analysis and phase noise (pnoise) analysis. The simulated ENF at 1 MHz offset frequency for the conventional TFB-VCO and the proposed PTFB-VCO are plotted in Fig. 7. It can be noticed that the simulation results for the power efficiency and ENF are in fair agreement with the analytical results obtained in Sect. 2.4. The simulated phase noises of the conventional TFB-VCO and the proposed PTFB-VCO at various conduction angle are also plotted in Figs. 8 (a) and (b), respectively. It was observed during the simulations that the conventional TFB-VCO fails to sustain oscillations (even when assisted start-up is provided by setting initial conditions) when the conduction angle is lowered below certain limits. In-order to reanimate the oscillator, the size of the tail transistor had to be increased. This results in an increase in the phase noise with lowering conduction angle as shown in Fig. 8 (a). On the other hand, the proposed PTFB-VCO successfully sustained oscillations at lower conduction angles without having to increase the tail transistor size, resulting in a lowering of phase noise with lower conduction angles, The simulation results also shows a lowering in flicker noise corner at lower conduction angles, which can be attributed to the lowering of the noise injection as hypothesized in Sect. 2.3, which is conceptually shown in Fig. 3 (b) [32]–[36].

3. Circuit Implementation

3.1 Principle of Operation

A pulse generator that satisfies the following requirements

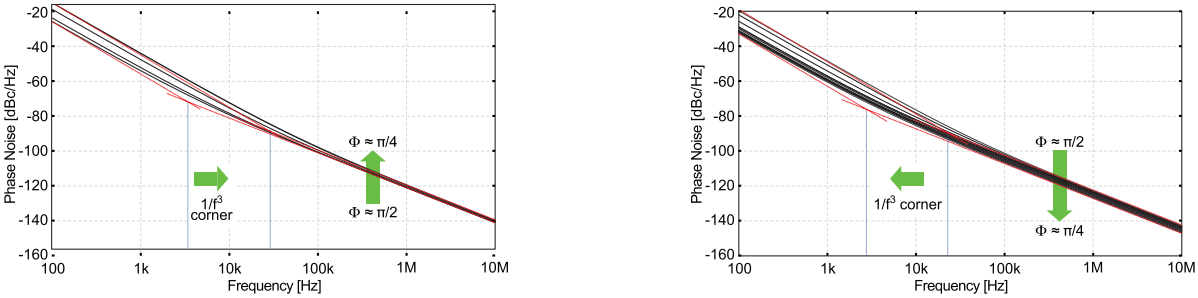


Fig. 8 Simulated phase noise of the (a) conventional tail-feedback VCO swept in the range of $\pi/2$ to $\pi/4$ and the proposed PTFB-VCO.

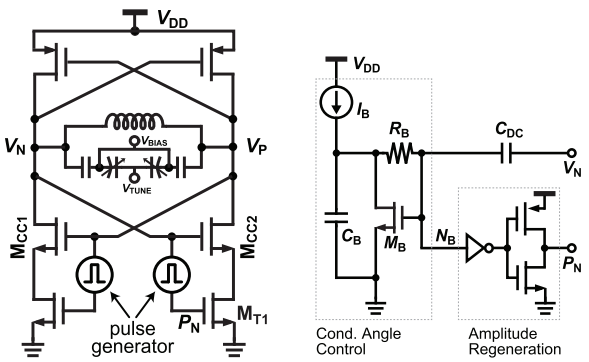


Fig. 9 Circuit schematic of (a) the proposed pulse-tail-feedback VCO (b) the proposed synchronized pulse generator.

is necessary to implement the pulse-tail-feedback VCO discussed in Sect. 2; (i) the generated pulse train must be synchronized to the VCO's tank oscillations, (ii) the generated pulses must possess large enough conduction angle (Φ) during the start-up phase of the VCO to ensure a robust oscillation buildup. and (iii) the conduction angle (Φ) must be kept lower than half a cycle of tank oscillation in steady state for minimizing the phase noise.

The proposed PTFB-VCO in Fig. 4 (c) is implemented in CMOS configuration as shown in Fig. 9 (a). The CMOS configuration is adopted for minimizing the power consumption for a given FoM [41]. Since the only fundamental difference between the circuit in Figs. 4 (c) and 9 (a) is the way in which the cross coupled pair is generating the required negative resistance, the analysis carried out in Sect. 2 holds for the CMOS version in Fig. 9 (a). A pulse generator circuit with adaptive pulse width control is proposed in this work for satisfying the above requirements, which is shown in Fig. 9 (b). The proposed pulse generator consists of two main modules, (i) a conduction angle control module, and (ii) an amplitude regeneration module. The working principle of the proposed pulse generator can be understood by studying Fig. 10 along with Fig. 9 (b). The oscillations in the VCO tank are sensed through the node V_N, which is then passed through a DC-block capacitor CDC. The signal present at node N_B is the vector sum of the AC and the DC signal generated by the bias network. The DC bias is generated using a current source I_B, a resistor R_B a capacitor C_B and a transistor M_B. Depending on the signal present at the node N_B, the pulse generator goes through three stages of operation as shown in Fig. 10; (i) start-up (ii) conduction angle reduction and (iii) steady state. During the start-up stage, there is no oscillations in the LC tank and as a result the AC voltage coupled to the node N_B is negligible. It can be noticed from Fig. 10 (a) that by applying an appropriate bias current, the voltage at N_B can be kept higher than the threshold voltage of the amplitude regeneration block. The amplitude regenerator then restores the voltage at P_N to the full supply level V_{DD}. This scheme ensures a highly robust start-up in class-A/AB mode. Once the oscillation builds up in the tank, the AC amplitude at N_B increases and as a result the operating condition of the transistor M_B alters between "off" and "on" states. This reduces the current flowing through the resistor R_B, which in turn reduces the DC voltage coupled to the node N_B. It can be observed from Fig. 10 (b) that this reduction in DC bias voltage results in a reduction in time for which the signal at the input of the amplitude regenerator $V(N_B)$ crosses its threshold voltage. Beyond this time point, the amplitude regenerator acts as pulse generator which is synchronized to the tank oscillations. The pulse width continues to reduce until the VCO achieves steady state, which is defined by the bias network as shown in Fig. 10 (c).

3.2 Challenges

As in any electronic circuitry, the implementation presented above faces challenges that must be solved for improving the VCO performance. A simplified circuit diagram of the proposed pulse-tail-feedback VCO is shown in Fig. 11 (a). In practice, the pulse generator will have an intrinsic delay (t_d), which results in a delay between the voltage signal at the gate of the tail transistor ($V_{g,t}$) and the gate of the cross coupled transistor ($V_{g,cc}$), a conceptual representation of which is shown in Fig. 11 (b). This means that the tail transistor enters full conduction while the cross coupled transistor pair is already moving towards cut-off. If the delay introduced by the pulse generator is excessively large, the

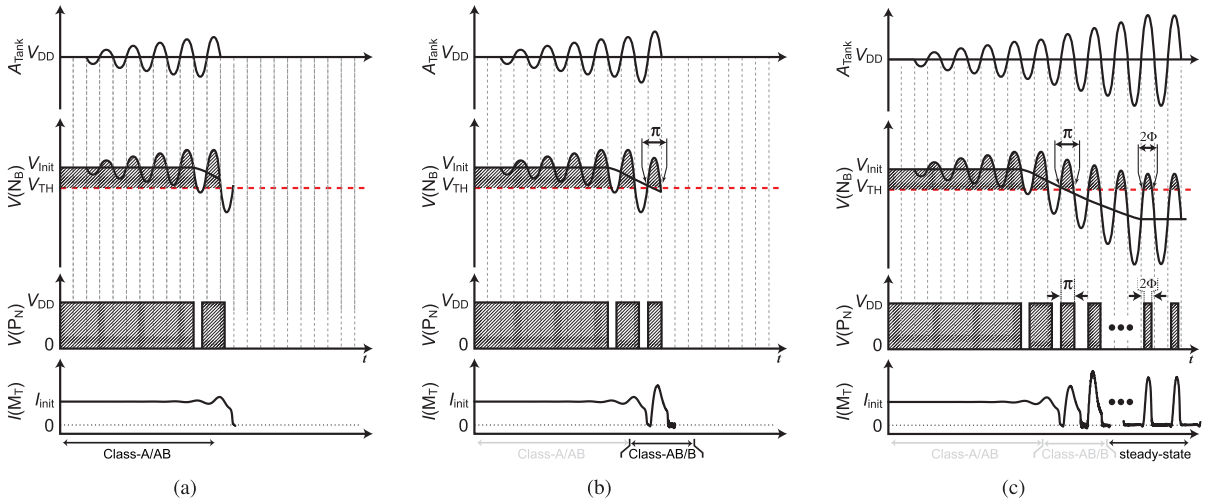


Fig. 10 Conceptual waveforms depicting the operating states of the proposed variable width pulse generator (a) start-up (b) pulse width reduction and (c) steady state along with the simulated current waveform at the tail transistor.

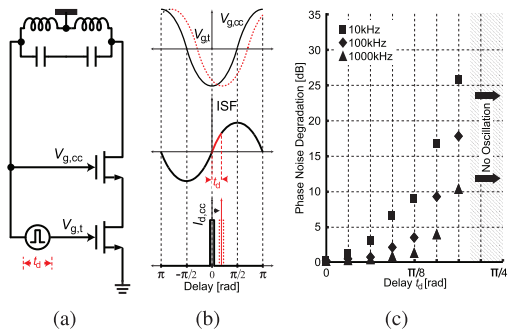


Fig. 11 Effects of the intrinsic delay of the pulse generator (a) simplified circuit diagram showing a single active branch of the proposed PTFB VCO (b) waveform showing the effects of delay on ISF (c) simulated phase noise degradation with increasing pulse generator delay.

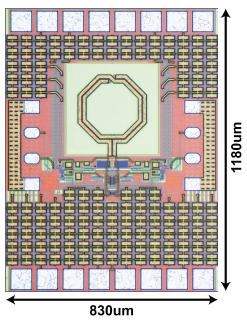


Fig. 12 Chip micrograph of the proposed pulse-tail-feedback VCO prototype.

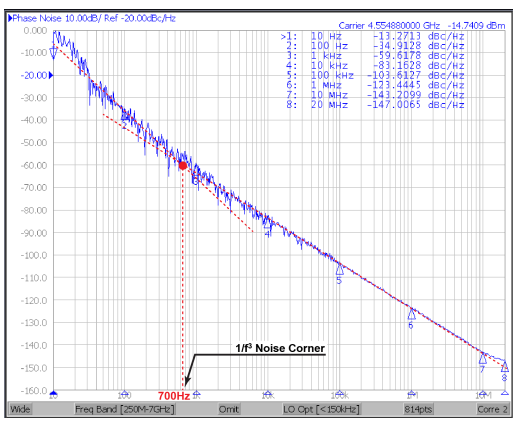


Fig. 13 Measured phase noise of the proposed PTFB VCO showing the flicker noise corner.

VCO might fail to sustain oscillations. On the other hand, if the delay is smaller, sustained oscillation is possible. However, the delay will have adverse effects on the phase noise. This reason for this is evident from the ISF theory [7]. The effect of pulse generator delay on the phase noise at various frequency offsets is simulated and is plotted in Fig. 11 (c). It can be noticed that the impact of t_d on the VCO phase noise is minimal at higher offset frequencies but increases substantially at lower offset frequencies. This is due to the increased flicker noise resulting from the inharmony in the current flowing in the LC-tank and the current flow in the cross coupled pair [24]. Even though this could be a limiting factor in certain scenarios, such challenges can be overcome by using advanced process nodes, increasing supply voltage, or by developing an improved pulse generator circuit.

4. Measurement Results

The proposed pulse VCO is fabricated in standard 180 nm CMOS process. The chip micrograph of the fabricated VCO is shown in Fig. 12. The chip size is 1180 µm × 830 µm with the VCO core occupying an area of 530 µm × 450 µm. The VCO oscillation frequency and output power are measured by a spectrum analyzer (Agilent E4407B ESA-E).

Figure 13 shows the phase noise measured by a signal source analyzer (Agilent E5052B SSA) at 4.55 GHz, while consuming 1.35 mW from a 1.2 V DC supply. Two

Table 1 Comparison of pulse-tail-feedback VCO with other low-flicker VCOs.

Reference	Frequency (GHz)	Power (mW)	Phase Noise(@1 kHz) dBc/Hz	(@10 kHz) dBc/Hz	(@1 MHz) dBc/Hz	FoM (@1 kHz) dBc/Hz	(@10 kHz) dBc/Hz	(@1 MHz) dBc/Hz	$1/f^3$ Corner (Hz)	Topology
[9]	4.9–5.5	1.3	−40.0*	−70.0*	−123.0*	176.6*	184.7	195.7	200,000	Class-C
[23]	4.7–5.4	0.50	−38.0*	−68.0*	−119.0	176.6*	184.7	195.0	200,000	CM-Resonance
[26]	5.4–7.0	10–12	−43.8*	−73.8	−124.5	170.7*	180.7	191.4	130,000	Class-F
[30]	2.4	4.20	–	−88.7	−128.4	–	190.1	189.8	-	Tail-Feedback
This Work	4.5–4.7	1.35	−-61.8**	−83.2	−123.4	**193.7**	195.1	195.3	**700**	Pulse-Tail-Feedback

* Calculated from the noise plot.
** Measured from averaged phase noise.

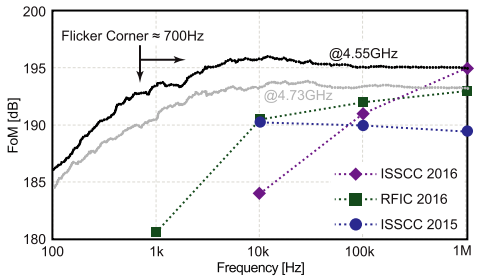
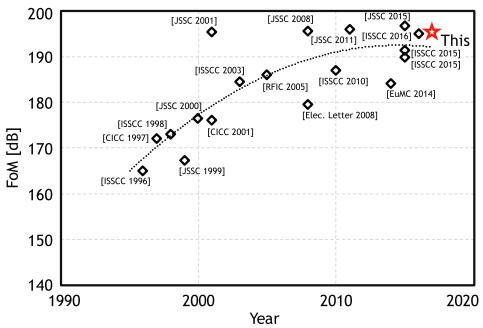
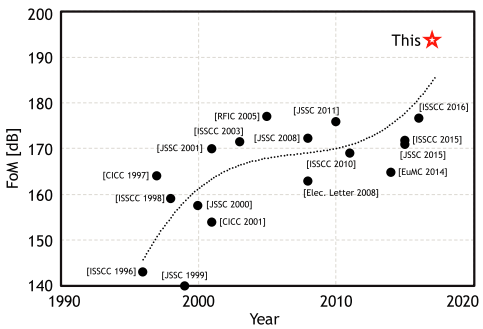


Fig. 14 Measured FoM of the proposed PTFB VCO compared with the recent VCOs employing state-of-the-art flicker reduction techniques.

lines with slopes of −30 dB/dec. and −20 dB/dec. (shown as dotted red lines) were overlapped on the measured phase noise plot for calculating the flicker noise. The intersection of these two lines mark the flicker corner frequency of 700 Hz. In order to visualize the effectiveness of the proposed pulse-bias technique and the importance of reducing the flicker corner, the figure-of-merit (FoM) of the VCO is calculated [5] and is shown in Fig. 14. The figure shows the FoM of the VCO at its lowest and highest operating frequencies of 4.55 GHz and 4.73 GHz respectively. It can be noticed from the plot that the at 4.55 GHz, the FoM maintains an average value of −195 dB/Hz after passing the flicker corner of 700 Hz. The pulse generator consumes 160 µW from 1.2 V supply, which degrades the FoM by approximately 1 dB. Comparing the FoM of the proposed PTFB-VCO with the other state-of-the art VCO designs utilizing flicker reduction techniques, it can be noticed that the proposed technique maintains relatively flat characteristics over a wider range of offset frequencies than the conventional works. From a PLL design perspective, this means that the proposed pulse-tail-feedback VCO can maintain an optimum power-jitter ratio over a wide range of PLL bandwidths. Figures 15 (a) and (b) compares the FoM of the proposed VCO with other high performance VCO designs at offset frequencies of 1 MHz and 1 kHz. It can be noticed from Fig. 15 (a) that the maximum achievable FoM beyond the flicker noise corner has stayed more or less the same from the year of 2001; thanks to the advancements in our understanding of the phase noise mechanism in VCOs [7]–[10], we now know that the maximum achievable FoM is bound by the quality (Q) factor of the tank and researchers were able to invent techniques that can achieve nearly ideal



(a)



(b)

Fig. 15 FoM (a) @1 MHz and (b) @1 kHz frequency offsets over the years.

FoM values. However, a quick look at the FoM plot for the 1 kHz offset, depicted in Fig. 15 (b) shows a stagnation in the flicker noise reduction for decades. The proposed technique achieves approximately 3 dB improvement in FoM at the 1 kHz offset as compared to the VCOs employing state-of-the-art flicker reduction techniques.

5. Conclusion

This paper proposes a pulse-tail-feedback technique for reducing the flicker noise in current-biased VCOs without compromising on the FoM. The proposed PTFB-VCO relies on reducing the current conduction period of the tail transistor and driving them into deep-triode region for reducing the noise generation and noise injection into the tank network. Theoretical analysis and extensive circuit-level simulations were carried out for validating the presented idea. A

prototype of the proposed PTFB-VCO is implemented in a standard 180 nm CMOS process. Laboratory measurements shows an improvement of approximately 4 dB at low frequency offset due to the very low flicker corner of 700 Hz. The low flicker corner helps the VCO to maintain an FoM of −195 dB within frequency offset ranging from 1 kHz to 10 MHz, which enables the VCO to be maintain consistent jitter-power performance when used in PLLs with widely different bandwidths.

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