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A Low-Jitter Injection-Locked Clock Multiplier Using 97-μW Transformer-Based VCO with 18-kHz Flicker Noise Corner

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SUMMARY This paper presents a high jitter performance injection-locked clock multiplier (ILCM) using an ultra-low power (ULP) voltage-controlled oscillator (VCO) for IoT application in 65-nm CMOS. The proposed transformer-based VCO achieves low flicker noise corner and sub-100 μW power consumption. Double cross-coupled NMOS transistors sharing the same current provide high transconductance. The network using high-Q factor transformer (TF) provides a large tank impedance to minimize the current requirement. Thanks to the low current bias with a small conduction angle in the ULP VCO design, the proposed TF-based VCO's flicker noise can be suppressed, and a good PN can be achieved in flicker region ($1/f^3$) with sub-100 μW power consumption. Thus, a high figure-of-merit (FoM) can be obtained at both 100 kHz and 1 MHz without additional inductor. The proposed VCO achieves phase noise of -94.5/-115.3 dBc/Hz at 100 kHz/1 MHz frequency offset with a 97 μW power consumption, which corresponds to a -193/-194 dBc/Hz VCO FoM at 2.62 GHz oscillation frequency. The measurement results show that the $1/f^3$ corner is below 60 kHz over the tuning range from 2.57 GHz to 3.40 GHz. Thanks to the proposed low power VCO, the total ILCM achieves 78 fs RMS jitter while using a high reference clock. A 960 fs RMS jitter can be achieved with a 40 MHz common reference and 107 μW corresponding power.

key words: *injection lock, frequency multiplier, IoT, ultra-low power, VCO, transformer, FoM, flicker noise, CMOS*

1. Introduction

Nowadays, the low jitter clock synthesizer is one of the most demanding components in various systems [1]–[4]. Those devices sustained by energy harvesters or low capacity battery must support low-voltage and low-power operation. That puts challenges on the clock synthesizer designs with considering the frequency tuning range (FTR), phase noise (PN) and power consumption. As one of the types of clock synthesizer, phase-locked loops (PLLs) based clock multipliers are commonly implemented in modern systems-on-chip, that multiply a low-frequency reference provided by a crystal oscillator. As we noticed, the commonly implemented type-II PLLs using low reference frequency can't provide sufficient voltage-controlled oscillator (VCO) noise suppression bandwidth, *e.g.,* <1 MHz, that protrudes the importance of $1/f$ (flicker) noise suppression in VCO, which degrades the close-in PN [5]. In contrast to PLLs, the injection-locked clock multipliers (ILCMs) lock oscillation frequency to an integer multiplier number of reference clock by injection pulses [3], [6]. In which, the noise performance of the VCO, including the flicker noise, has significant influence on the ILCM's phase noise performance.

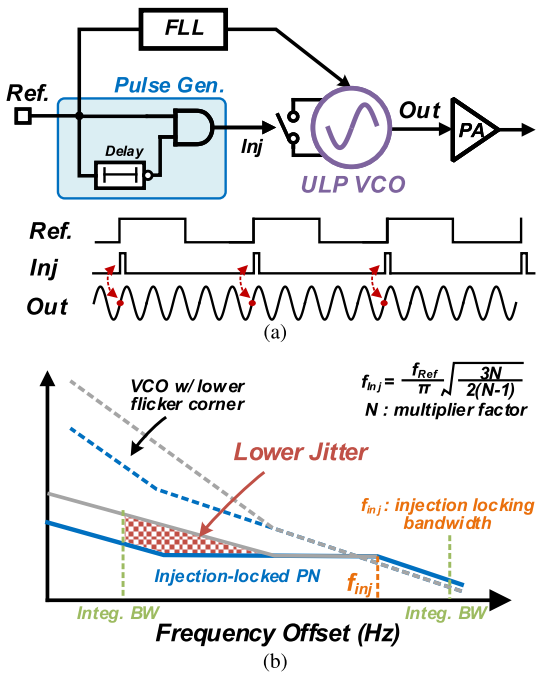

Fig. 1 (a) Injection-locked frequency generator and its time-domain waveform during injection for frequency multiplication. (b) Lower jitter with good flicker corner.

Forwarding the reference frequency and injecting it directly into the VCO has been used to improve jitter performance of the VCOs [7]–[12], which has lower power consumption benefiting from its simply structure. The conventional ILCM is shown in Fig. 1(a). By correcting the oscillator zero crossings periodically using the pulse generated from a low jitter reference, the jitter accumulation can be lowered [13]. And a good in-band phase noise can be achieved thanks to the wide noise suppression bandwidth as shown in Fig. 1(b). According to phase noise analysis in [14], the single sideband phase noise $\mathcal{L}_{\mathrm{IL}}(f)$ of injection-locked clock multiplier based on a VCO is given as

$$\mathcal{L}_{\mathrm{IL}}(f) = \mathcal{L}_{\mathrm{VCO}} \cdot \frac{2\pi^2(N-1)(2N-1)}{3f_{\mathrm{ref}}N^2} \cdot \frac{f^2}{1+(\frac{f}{f_{\mathrm{inj}}})^2} \quad (1)$$

where f_{ref} is the injection reference, N is the multiplication

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factor and the f_{inj} is the injection locking bandwidth which can be expressed as

$$f_{inj} = f_{ref} \cdot \frac{1}{\pi} \cdot \sqrt{\frac{3N}{2(N-1)}} \quad (2)$$

Based on the Eq. (1) and (2), several inspections can be observed. First, the in-band phase noise will experience a 1st-order suppression with a wide bandwidth f_{inj}, which is close to 0.4 times f_{ref}. Thus, with a high reference frequency and a small value of N, a wide noise suppression bandwidth f_{inj} is available. Meanwhile, at the high offset frequency, the phase noise of the injection-locked VCO is 3 dB higher than the free-running VCO. Thus, according to the above points, a low-power VCO with a good $1/f^2$ noise performance is a suitable candidate to be the high jitter performance (*e.g.* < 100 fs) ILCM with the assistance from a high reference frequency. However, it is worth noting that the noise degradation in injection-locked frequency generator due to the flicker noise is also significant, because of the injection lock operation can only suppress the VCO noise by 1st-order (2nd-order in conventional type-II PLL). A VCO with low flicker corner and low $1/f^2$ noise is superior compared with the one with bad phase noise performance. The Fig. 2 shows the calculated jitter performance of the ILCM with different VCO flicker corner. In case of a 40 MHz reference frequency, a VCO flicker corner lower than 100 kHz is desired to minimize the integrated RMS jitter with a ultra-low power consumption. In addition to using a higher injection frequency, such as 80 MHz or higher, a LC-VCO, which has both good flicker noise and thermal noise performances, is attractive for high jitter performance ILCM implementation.

As CMOS scales, the MOS transistor's flicker noise will further degrade the close-in PN, thus limiting the achievable jitter performance of the PLL or ILCM and the data rate of transceiver finally. Since the tail filter technique [15] firstly introduced in CMOS oscillators to suppress the $1/f$ upconversion from the current source, many efforts has been made to reducing the $1/f$ upconversion mechanisms through dedicated design techniques [16]–[20]. It is worth noting that these designs operate with larger than 0.3 mW power consumption. With a limited current from a low supply voltage, cross-coupled transistors with large size can provide a sufficient G_m. However, it should be noticed that the non-linear gate capacitance of the oversize transistor will increase the harmonic power and aggravate the flicker upconversion. Since the FoM is a function of the power dissipation and the achievable phase noise performance. The VCO with ultra-low power consumption and good phase noise performance also can achieve good FoM and be attractive for the low-power applications, such as digital PLL [21], [22] and BLE transceivers [23], [24]. Also, as indicated in [25], the open-loop operation of VCO can be helpful in saving TX power which requires VCO to have both low $1/f^3$ and $1/f^2$ phase noise.

In this paper, a sub-100 µW VCO based on a single transformer structure is proposed with low flicker noise corner and ultra-low power consumption, which is extended version of [26]. The analysis of the transformer-based tank impedance, startup condition, and flicker noise is firstly added in this work and verified with more detailed simulation/measurement results. To verify the high performances of the VCO, a low-power ILCM is built based on this ULP VCO targeting for high jitter performance (*e.g.* <100 fs) with a sub-300 µW power consumption.

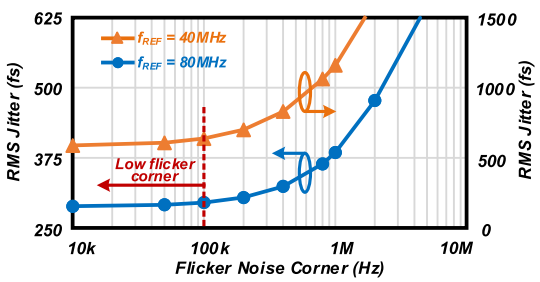

Fig. 2 Calculated jitter performance of ILCM with different VCO flicker corner.

2. Transformer-Based ULP VCO

The diagram of the proposed VCO is shown in Fig. 3. To achieve good PN performance with a low power consumption, high-Q factor transformer using co-planar structure is implemented in the load tank with minimized on-chip area and minimum number of cross-sections. Also, the capacitor bank can be designed with small tuning range which has a high quality factor (> 50) because of the large inductance of TF. Thus, the quality factor of the tank is mainly dominated by the transformer. Through the center tap of both swings, DC current is shared by the two cross-coupled NMOS transistor to provide sufficient mobility. The large inductance of the secondary swing L_S and passive gain in TF ensure the start-up with small current bias. Both the supply port and ground port are at the bottom side of the transformer, which provides a well-defined common-mode return path.

The noise of the tail current source can appear as a CM signal and modulate the oscillation voltage. This phe-

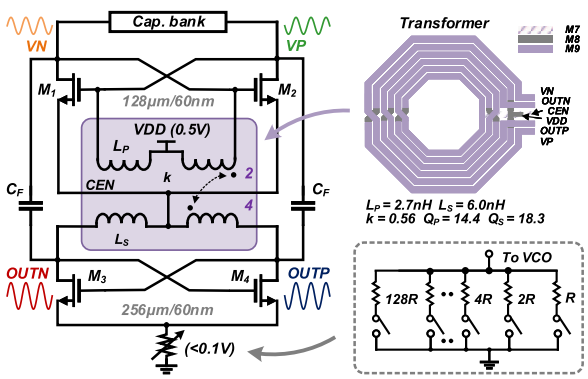

Fig. 3 Proposed ULP transformer-based VCO with flicker noise reduction.

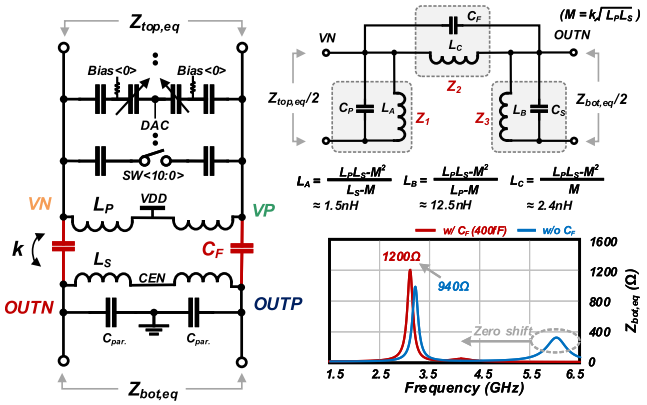

Fig. 4 Schematic of capacitor bank and equivalent model of the half transformer.

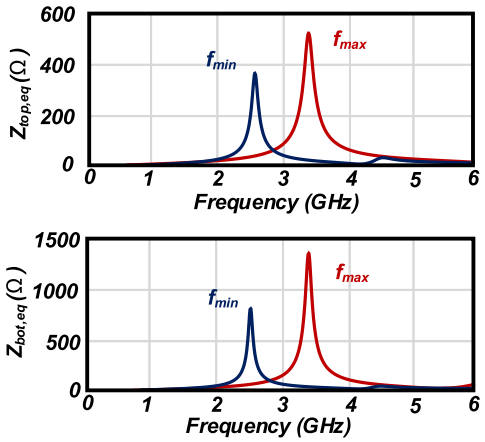

Fig. 5 Simulated tank impedance over frequency tuning range.

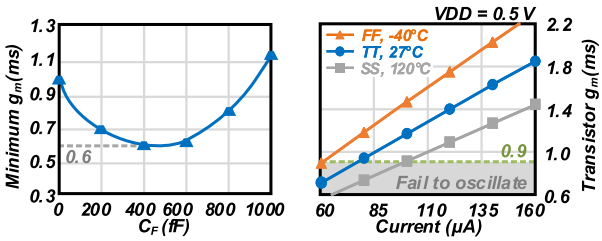

Fig. 6 Calculated minimum required g_{m0} and simulated transistor g_{m0} versus different current bias.

nomenon will become more serious when insufficient voltage headroom is added on the current source [22]. Also, to mitigate the voltage drop from the current source, which degrades the voltage efficiency, an 8-bit binary resistor bank is implemented for the current control with the range from 90 μA to 360 μA.

2.1 Transformer-Based Tank and Start-Up Condition

Figure 4 shows the implemented transformer-based network with capacitor banks. A 6-bit switchable capacitor bank is implemented for coarse frequency tuning, and a 9-bit linearized varactor is used for fine frequency tuning. As derived in [22], the load impedance transfer ratio can be expressed as the turn ratio L_P:L_S and the start-up condition can be written as:

$$g_{m0} > 2/(1 + L_P/L_S)Z_{bot,eq} \tag{3}$$

In which, $Z_{bot,eq}$ represents the input impedance from the bottom side of the transformer and all the transistors (M1~M4) have the same g_{m0} at start-up condition.

To clearly show the TF's impedance with additional C_F, half circuit of the transformer including the VN port and OUTN port is analyzed, and the conventional T equivalent model is converted to π equivalent model using Wye-Delta Transformation [27]. Compared with T-model, the π-model shows better terminal behavior when a large leakage inductance appears [28]. The Z_1, Z_2, and Z_3 represent the parallel resonance impedance of each part in π equivalent network, as shown in Fig. 4. The $Z_{bot,eq}/2$ can also be expressed as the $Z_3 \parallel (Z_2 + Z_1)$. Due to the limited coupling factor k (<0.6) from the multi-turns co-planar TF structure, a large L_C appears (≈ 2.4 nH), which degrade the parallel impedance. An appropriate zero-shifting capacitance C_F [29], which resonate with L_C at fundamental frequency, can maximize $Z_{bot,eq}$ value with a slight frequency drift. It needs to notice that the parasitic capacitance between two windings should also be considered as a additional part of C_F. To obtain a maximized impedance from bottom-side ($Z_{bot,eq}$), both of (Z_1+Z_2) and Z_3 should be maximized. In which, the value of (Z_1+Z_2) will be havily infulence by the Z_2, which is the parallel resonate impedance of L_C and C_F. Also, because of the complexity of the actual TF model, The optimal value of C_F can only be obtained by simulation. In simulation, a 400 fF of C_F can improve the peak impedance of $Z_{bot,eq}$ from 940 Ω to 1200 Ω which can reduce the minimum current required at the start-up condition. The simulated results of both top and bottom ports are shown in Fig. 5. To simulate the input impedance from the bottom-side and up-side respectively, a 50 Ω port is placed in one of the ports while the other one is floating. Note that both of the parasitic capacitance from transistors should be considered as a fixed part of the capacitor bank. The maximum oscillation frequency is achieved with capacitor bank is turned off with approximately 210 fF capacitance, while the minimum oscillation frequency can be obtained with all the capacitors are turned on. Thanks the high impedance $Z_{bot,eq}$ provide by this tank, the minimum required start-up g_{m0} can be minimized and a robust oscillation startup can be realized.

Figure 6 shows the calculated minimum required g_{m0} and simulated transistor g_m versus different current bias. In simulation, a 90 μA current with 0.9 mS g_{m0} is sufficient to sustain the oscillation with a slow-slow (SS) corner (120 °C). In the post-layout simulation, larger than 300 mV oscillation amplitude is confirmed in all PVT corners with same bias current (190 μA) from 0.5 V DC supply.

2.2 Low Flicker Noise Corner

Since the low-power startup benefits from the cooperation of the large NMOS transistors and high tank impedance, the flicker noise upconversion is also mitigated from a small conduction angle with a low-power consumption. According to the impulse sensitivity function (ISF) theory [30], the flicker noise upconversion in cross-coupled oscillation involves the following steps. First, the flicker noise, in voltage $v_{1/f}$, at the offset frequency $\Delta\omega$ will be modulated to current noise around different harmonics $k\omega_0 \pm \Delta\omega$ through a noise modulation function (NMF), which is once determined by the transistor's time-varying transconductance $G_{\mathrm{m}}(t)$. It should be noted that a more accurate NMF should be utilized with the consideration of the correlated mobility fluctuation (CMF) [5], which is also influenced by the drain current I_{D} in advanced technology. The NMF can be described as

$$m(t) = G_{\mathrm{m}}(t) + \Omega I_{\mathrm{D}}(t) \tag{4}$$

where $m(t)$ is the NMF. Ω is the process parameter, which is the function of Coulomb scattering coefficients, the volumetric oxide trap density, and oxide capacitance per unit area of the interfaces [31]. $G_{\mathrm{m}}(t)$ and $I_{\mathrm{D}}(t)$ are the steady-state waveform which can be obtained by the transient simulation in Spectre. The flicker current noise can be written as

$$i_{1/f}(t) = v_{1/f}(t) \times m(t) \tag{5}$$

Assuming the $v_{1/f}(t)$ at $\Delta\omega$ is expressed as $v_{1/f}(t) = \sqrt{2}V_{1/f,RMS}\cos(\Delta\omega t + \gamma)$, in which the γ is an initial random phase. The current noise can be rewritten as

$$i_{1/f}(t) = \sqrt{2}V_{1/f,RMS} \times m(t) \times \cos(\Delta\omega t + \gamma) \tag{6}$$

$$= \sqrt{2}I_{1/f,RMS}\cos(\Delta\omega t + \gamma) \tag{7}$$

Though the $I_{1/f,RMS}$ can be directly obtained by the periodic steady-state (PSS) simulation in Spectre, the understanding of how the $m(t)$ influences the $I_{1/f,RMS}$ can give us the guideline to design the VCO with lower flicker noise corner. According to [31], the term of ΩI_{D} is relatively small compared with the G_{m}, due to the small CMF factor Ω in 65 nm node and low current bias. Therefore, it should be noted that $G_{\mathrm{m}}(t)$ will dominate the $m(t)$ and mainly considered here.

Secondly, the flicker noise current will converted to phase noise through its corresponding ISF, and the non-normalized ISF can be expressed as

$$h_{\mathrm{DS}}(t) = \frac{1}{2}h_0\cos\theta_0 + \sum_{1}^{N}(h_k\cos k\omega_0 t + \theta_k) \tag{8}$$

where h_{k} is the magnitude of the ISF at each harmonic and its corresponding phase θ_k. Both the h_{k} and θ_k can be estimated by using the simulator PSS and PNOISE in Spectre. Finally, the single-sideband to carrier ratio (SSCR) can be expressed using the non-normalized effective ISF ($h_{eff}(t)$) as

$$\mathcal{L}_{\Delta\omega} = 2\left(\frac{\sqrt{2}}{2\Delta\omega}\cdot h_{eff}(t)\right)^2 \tag{9}$$

$$= 2\left(\frac{\sqrt{2}}{2\Delta\omega}\cdot\frac{1}{T}\int_0^T h_{\mathrm{DS}}(t)\cdot I_{1/f,RMS}(t)dt\right)^2 \tag{10}$$

From equation (10), two approaches are indicated to minimize the flicker noise corner. One is to make the $h_{\mathrm{DS}}(t)$ more symmetrical and narrow the upper and lower ranges, such as increasing the quality factor of the tank or reducing the even harmonic components. Another way is to reduce the absolute value of the $I_{1/f,RMS}$, such as increasing the transistor gate size (lower $V_{1/f,RMS}$) and narrow the conduction angle (lower $m(t)$).

In general, the flicker noise current will modulate the waveform within a window $m(t)$ determined by current and transconductance which influenced by the transistor's conduction angle. Thus, to reduce the flicker noise upconversion, one way is directly reduce the flicker noise current which associated with transistor's gate area. And another way is to reduce the conduction-angle (*i.e.,* class-C VCO) which also means to narrow the noise modulation window [20]. What should be noticed here is that to reduce the conductance angle in steady-state, the current bias must be relatively small to avoid large voltage waveform. However, the small current bias will also lead to small mean value of transconductance, which makes the startup become more difficult [32].

Figure 7(a) shows the simulated waveforms of top transistor M2 and bottom transistor M4. Due to the low supply voltage (*i.e.,* 0.5 V), which shared by the stacked structure, and the low current bias condition, the gate voltage waveform of bottom transistors is lower than the threshold voltage at the most of the time. Thus, the bottom transistor cross-coupled pair works most of time in class-C region with small conduction-angle ($\approx 90°$). Meanwhile, the top cross-coupled pair works with a relatively larger conduction-angle ($\approx 120°$). The flicker noise contribution from both top and bottom transistors will be mitigated. The DC value of the impulse sensitivity function accounts for the flicker noise upconversion. To verify the different current cases, both ISF and flicker noise current simulations are carried out with different current conditions. Figure 7(b) shows the simulated ISF functions with different current condition for both transistors M2 and M4. Figure 7(c) shows the simulated the RMS value of flicker noise current of both upper and lower transistors. With a large current which leads a large conduction angle, the flicker noise current will increase as the red dot line shown in Fig. 7(c). Meanwhile, a small transistor size will also contribute a larger flicker noise component. As shown in Fig. 7(d), the effective non-normalized ISF function of M2 transistor is also small thanks to the large transistor size (128 µm/60 nm), which reduces the absolute flicker noise current. Meanwhile, the bottom transistor M4 has as a much lower DC value of ISF function thanks to the narrow conduction angle with a proper current biasing. The

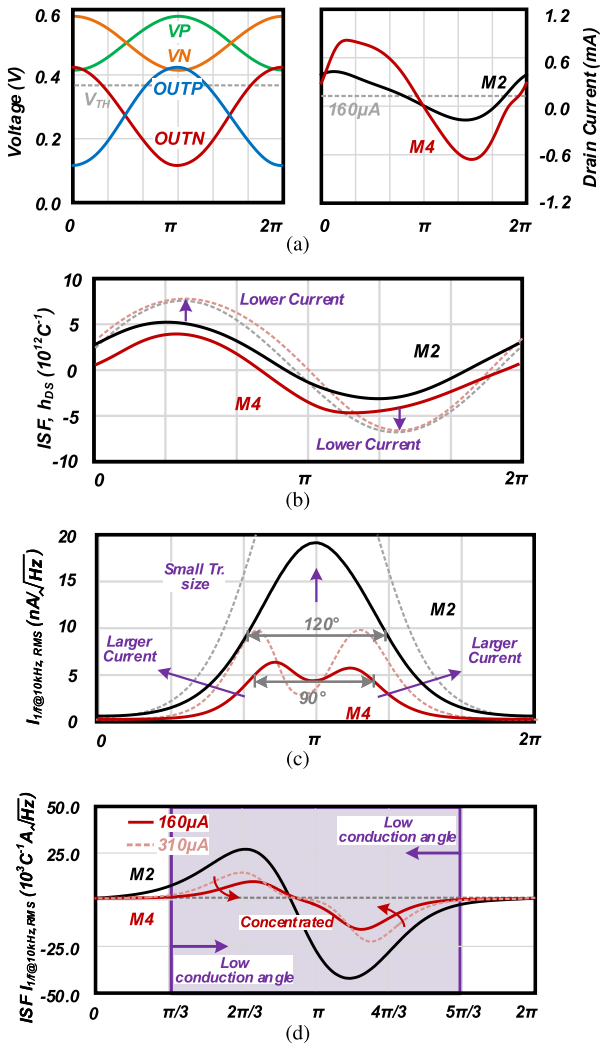

Fig. 7 (a) Simulated waveforms of V_{GS}, V_{DS}, and drain current I_D of transistor M2 and M4. (b) Simulated Non-normalized ISF functions of M2 and M4. (c) Modulated RMS value of flicker current noise at 10 kHz of M2 and M4. (d) Simulated effective non-normalized ISF function with different current bias (160/310 μA).

resistor bank only degrades the $1/f^2$ phase noise in a small value (< 5%) and has negligible impact on the flicker corner.

2.3 ILCM Implementation

To indicate the performances of the proposed VCO, a ILCM diagram with a integer mode is constructed as shown in Fig. 8. Note that the power consumption of the VCO core and the pulse generator are commonly considered in the ILCM designs and higher reference frequency will inevitably increase the power consumption of the pulse generator.

The pulse generator generates narrow pulse with adjustable pulse width using the positive edges of the reference clock and the generated pulses are injected into the TF-based VCO through an NMOS transistor [33]. The pulse width can be adjusted from 45 ps to 186 ps using a

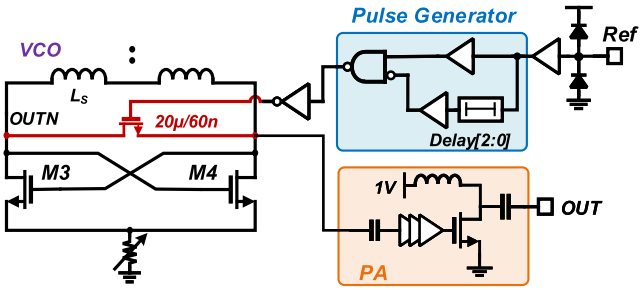

Fig. 8 ILCM implementation with pulse generator and test buffer.

3-bit delay control word with a 1-V power supply in post-layout simulation. A 20 μm/60 nm NMOS transistor is implemented as the shunt transistor for the pulse injection. It should be noticed that the injection from the bottom side of the VCO has a much more obvious effect because the larger differential waveform amplitude. A inverter driven common source power amplifier is constructed as the test buffer. The first stage of the VCO buffer is using a resistor feedback low-VT inverter.

3. Measurement

Figure 9 shows the die micrograph. The VCO is implemented in TSMC 65 nm 1P9M CMOS technology with one ultra-thick top metal layer, and the core area is 0.28 mm^2 which mostly occupied by the single transformer. To generate the injection pulse, the implemented pulse generator is constructed using the standard digital logic cells in the 65-nm CMOS process. A inverter driven common-source power amplifier (PA) is implemented for the phase noise measurement. To mitigate the influence of electromagnetic coupling between the PA and the transformer, a vertically symmetrical layout is employed.

3.1 ULP VCO Measurement

The phase noise is tested with signal source analyzer (Keysight E5052B) and Fig. 10 shows the measured PN at 100 kHz, 1 MHz, and 10 MHz, at 2.62 GHz oscillation frequency. In measurement, two external low-dropout linear voltage regulators (LDOs) are utilized to provide an ultra-low-noise DC supply and frequency tuning voltage, respectively. Fine current control can be realized with the on-chip 8-bit resistor bank, which is added in the tail of VCO. The measured $1/f^3$ corner is 18 kHz with drawing 194 μA current from 0.5 V DC supply. Meanwhile, this proposed TF-based VCO achieves -94.5/-115.3 dBc/Hz at 100 kHz/1 MHz frequency offset, corresponding to a -193/-194 dBc/Hz VCO FoM. The difference in FoM at 100 kHz and 1 MHz is less than 1 dBc/Hz thanks to the low $1/f^3$ corner achieved in this design.

The PN plots at representative oscillation frequencies are shown in Fig. 11. The phase noise variation is lower than 4.5 dB over the frequency tuning range (FTR) from 2.57 GHz to 3.40 GHz with a peak FoM -194 dBc/Hz. The

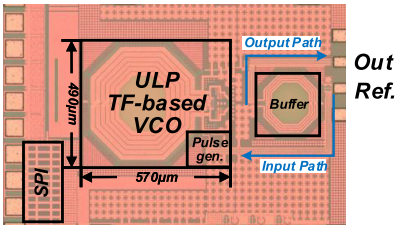

Fig. 9 Chip micrograph.

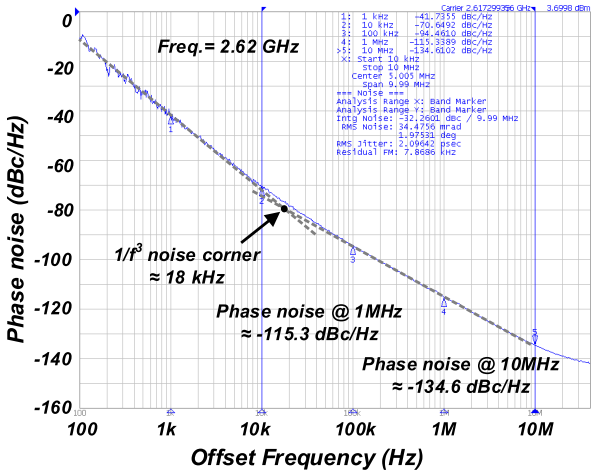

Fig. 10 Measured phase noise of the VCO at 2.62 GHz oscillation frequency.

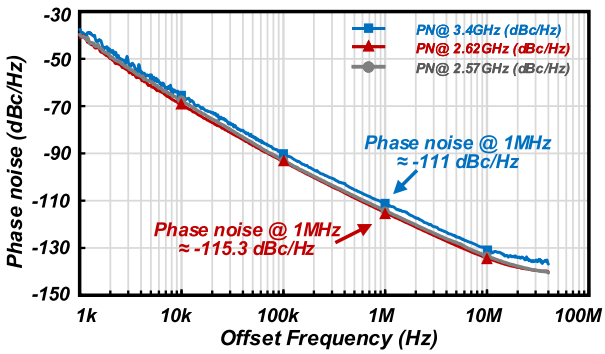

Fig. 11 Measured phase noise of the VCO at representative frequencies.

measured flicker noise corners over the frequency tuning range are shown in Fig. 12. The $1/f^3$ corner is below 60 kHz over the tuning range and better flicker noise performance achieved with lower oscillation frequency. The phase noise and FoM over the frequency tuning range are summarized in Fig. 13. Figure 13(a) shows PN at 100 kHz and 1 MHz, respectively versus different oscillation frequencies. Figure 13(b) shows the corresponding FoM versus oscillation frequencies and the FoM achieves below -190 dBc/Hz over the tuning range thanks to good phase noise performance with low power consumption. The measured VCO supply sensitivity K_{VDD} is around 270 MHz/V at 0.5 V supply voltage due to the large size of transistors working in the current limited region. Figure 14 summarizes the power and

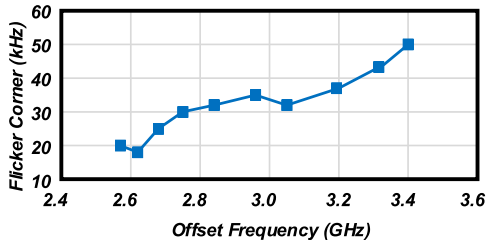

Fig. 12 Measured flicker noise corner over the frequency tuning range frequencies.

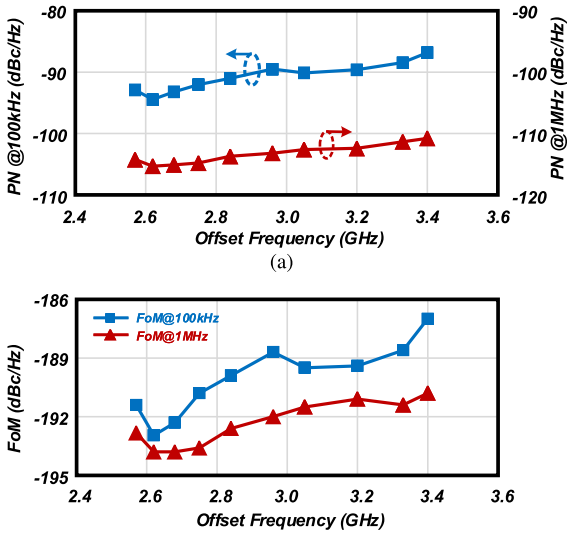

Fig. 13 (a) Phase noise (b) FoM at 100 kHz and 1 MHz over the frequency tuning range frequencies.

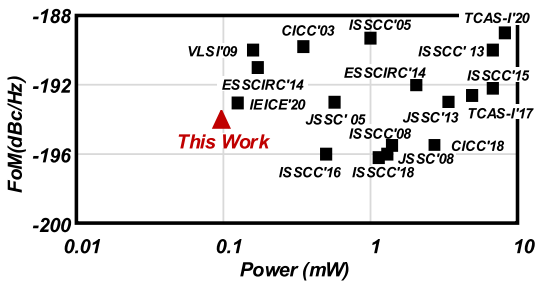

Fig. 14 The comparison of power and FoM in low-power LC-VCOs.

FoM of the low-power LC-VCO designs. This work breakthrough the sub-100 μW power barrier and achieves best FoM around the left corner in the FoM Summary. The performance of the proposed VCO is summarized and compared with state-of-the-art VCO in CMOS processes, as shown in Table 1. Compared to other VCOs, this design achieves both low flicker corner and a good $1/f^2$ phase noise performance with an ultra-low power consumption.

3.2 ILCM Measurement

Figure 15 shows the measured injection-locked phase noise

Table 1 Performance comparison with state-of-the-art oscillators

		This Work	[18]	[20]	JSSC'13	[17]	[19]	[16]	VLSI'09
Tech. (nm)		65	28	28	65	65	40	130	180
Architecture		Implicit Resonate	Implicit Resonate	Conduct Angle Reduction	Drain Resistor	Inverse Class-F	Implicit Resonate	Noise Circulating	Dual Class-C
VDD		0.5	0.7	0.3	1.2	0.6	1.0	1.2	0.2
Tuning Range (GHz)		2.57~3.40 (27.8%)	4.7~5.4 (13.8%)	2.02~2.87 (35%)	3.3~3.6 (18.2%)	3.49~4.51 (25.5)	5.4~7 (25.8%)	2.04~2.47 (19%)	N.A.
Power (mW)		0.097	0.5	0.75	0.72	1.14	10	2.58	0.114
Osc. Frequency (GHz)		2.62	4.7~5.4	2.4	3.3	4.51	7	2.35	4.5
Phase Noise (dBc/Hz)	100 kHz	-94.5	-108	-95.9	-47@1 kHz	-98.5	-102.1	-109.8	-79
	1 MHz	-115.2	-131	-119.3	-114	-143.7	-124.5	-131.6	-104
FoM_{VCO}* (dBc/Hz)	100 kHz	-193	-193 (@200 kHz)	-184.8	-179@1 kHz	-191	-188.9	-193.1	-181
	1 MHz	-194	-196 (@5 MHz)	-188.1	-189.8	-196.2	-191.4	-195.6	-187
Flicker Noise Corner (kHz)		18~50	200	60~100	N.A.	300	60	50	200~300
TF/Inductor Count		1	1	1	1	1	1	1	1
Area (mm^2)		0.28	0.18	0.14	0.08	0.22	0.13	0.36	0.19

* $FoM_{VCO} = \mathcal{L}(f_{offset})$ - 20log(f_0/f_{offset}) + 10log(P_{DC}/1 mW)

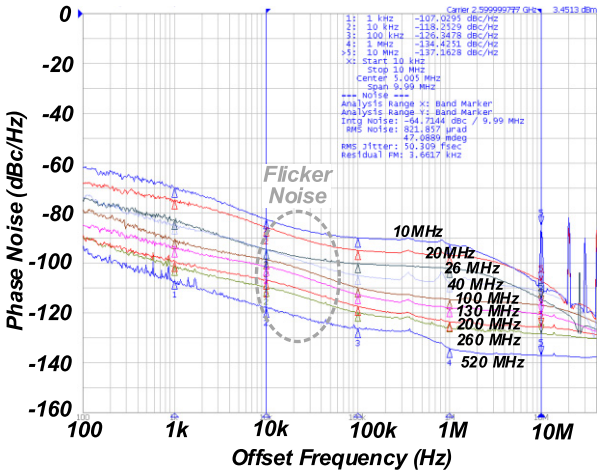

Fig. 15 Measured injection-locked phase noise with different reference frequencies.

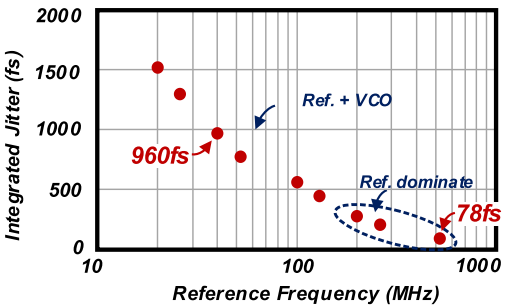

Fig. 16 Measured integrated jitter performance.

with different reference frequencies. The ILCM is fabricated in 65-nm CMOS technology. At the 2.6 GHz operation frequency, the available injection ratio ranges from 5 to 260, corresponding to the power consumption from the 210 μW to 107 μW.

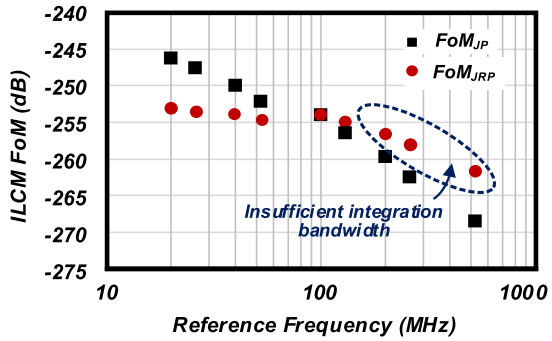

Fig. 17 Calculated FoM with different injection reference frequencies.

As shown in Fig. 16, a 78 fs integrated RMS jitter (10 kHz to 40 MHz) can be achieved with a 520-MHz reference. With a 40 MHz common reference, a 960 fs RMS jitter can be achieved with 107 μW corresponding power. Figure 17 plots the calculated jitter-power FoM (FoM_{JP}), where

$$FoM_{JP} = 10\log_{10}\left\{\frac{Jitter^2}{(1\,s)^2}\cdot\frac{Power}{1\,mW}\right\} \quad (11)$$

The FoM with consider reference frequency, FoM_{JRP}, can be written as [34], where

$$FoM_{JRP} = 10\log_{10}\left\{\frac{Jitter^2}{(1\,s)^2}\cdot\frac{Power}{1\,mW}\cdot\frac{f_{ref}}{100\,MHz}\right\} \quad (12)$$

In which, the f_{ref} represents the frequency of reference clock. Figure 18 compares the measured jitter performance and the power consumption of the proposed ILCM with state-of-the-art low-jitter PLLs. Table 1 summarizes the proposed ILCM performance and shows a performance comparison with the other works. This work achieves -50 dBc reference spur in measurement which can be potentially satisfy some wireless transceivers, such as Bluetooth Low-Energy which requires a spur level lower than -40 dBc above

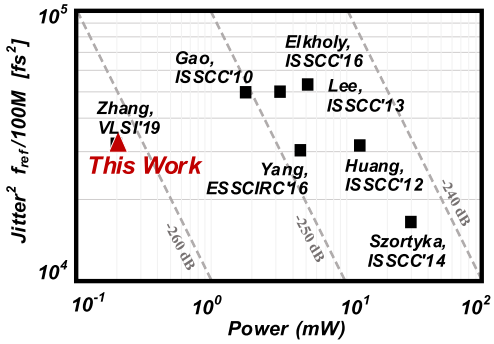

Fig. 18 State-of-the-art ILCMs.

Table 2 Comparison with state-of-the-art works.

Reference	[7]	[10]	ISSCC'14	[34]	This Work
Architecture	Int.-N ILCM	Int.-N ILCM	Int.-N ILCM	Int.-N ILCM	Int.-N ILCM
Technology [nm]	65	65	65	65	65
Freq. Range [GHz]	0.5-1.6	6.75-8.25	2.4	2.2-2.6	2.57-3.40
Multi. Factor [N]	4-30	64	16	3-24	5-260
Ref. Frequency [MHz]	40-300	105-129	150	100-800	10-520
RMS Jitter [fs] @ Ref. [Hz] (Int. Range [Hz])	700 @300M (10k-40M)	184 @106.25M (10k-100M)	188 @150M (1k-40M)	70 @800M (10k-40M)	78 @520M (10k-40M)
Ref. Spur [dBc]	-46	-40	-49	-66	-50
Power [mW]	0.97	2.25*	5.2*	0.2	0.21
Area [mm^2]	0.022	0.25	0.12	0.25	0.28
FoM$_{JP}$ [dB]	-243	-251	-247	-270	-269
FoM$_{JRP}$ [dB]	-239	-251	-246	-261	-262

* Total power of PLL, including the buffer and digital.

3 MHz frequency offset [24]. Compared with [34], this work has a worse reference spur level due to the lack of PLL which helps in injection timing optimization. To improve the reference spur performance, a continuous frequency tracking loop with a gated option can be implemented to optimize the injection timing with PVT variations [10], [35].

4. Conclusion

An ultra-low-power TF-based VCO with flicker noise reduction and good $1/f^2$ phase noise is proposed for IoT application. The transformer-based network provides a large tank impedance with the assistance from the inserted capacitor. Thanks to the high-quality factor with large tank impedance, the proposed VCO achieves -115.3 dBc/Hz phase noise at 1 MHz frequency offset while only consumes 97 μW power, which corresponds to a -194 dBc/Hz FoM. Meanwhile, an 18 kHz flicker noise corner is achieved with small current bias and conduction angle reduction, and $1/f^3$ corner is below 60 kHz over the wide tuning range from 2.57 GHz to 3.40 GHz. The proposed ULP TF-based VCO proves its feasibility in low power consumption applications with a low reference frequency. The total power of ILCM can be reduced to 107 μW, while 960 fs RMS jitter and -254 dB FoM$_{JRP}$ can be achieved with a 2.6 GHz operating frequency using a 40 MHz input reference clock. A 78 fs RMS jitter is also available with a 520 MHz input reference clock. The proposed ILCM demonstrates its applicability in high jitter performance and low-power clock generator applications.

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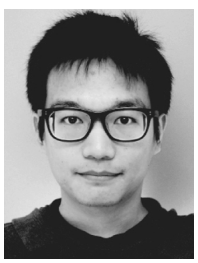

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