INVITED PAPER *Special Section on Analog Circuits and Their Application Technologies*

Analysis and Design of Continuous-Time Comparator

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SUMMARY Applications of continuous-time (CT) comparator include relaxation oscillators, pulse width modulators, and so on. CT comparator receives a differential input and outputs a strobe ideally when the differential input crosses zero. Unlike the DT comparators with positive feedback circuit, amplifiers consuming static power must be employed in CT comparators to amplify the input signal. Therefore, minimization of comparator delay under the constraint of power consumption often becomes an issue. This paper analyzes transient behavior of a CT comparator. Using "constant delay approximation", the comparator delay is derived as a function of input slew rate, number of stages of the preamplifier, and device parameters in each block. This paper also discusses optimum design of the CT comparator. The condition for minimum comparator delay is derived with keeping power consumption constant. The results include that the optimum DC gain of the preamplifier is e~e^3 per stage depending on the element which dominates load capacitance of the preamplifier.

key words: *comparator, continuous time, analysis, optimization, relaxation oscillator, pulse width modulator, single-slope A/D converter*

1. Introduction

Applications of continuous-time (CT) comparator include relaxation oscillators [1], pulse width modulators [2], and single-slope A/D converters [3]. Examples of their configurations and waveforms are shown in Fig. 1. In these applications, the delay of the CT comparator t_d causes errors in oscillation frequency, duty cycle, and A/D conversion result. Although some of these errors can be calibrated (e.g., by applying an intentional offset to the comparator), post-calibration drift caused by variations of temperature and supply voltage often becomes a problem. This drift can be minimized by making the original delay shorter. Therefore, the reduction of the comparator delay is one of the keys for realizing these systems.

This paper analyzes transient behavior of the CT comparator and discusses its optimum design. In the next section, CT comparator and discrete time (DT) comparator are compared. In Sect. 3 two examples of CT comparator are simulated and role of the preamplifier is investigated in advance of analysis. Section 4 derives an approximation formula that describes the delay of the CT comparator having a multi-stage preamplifier with a differential/single-end signal converter and a common-source inverter in the backend. Section 5 discusses optimum designs of the CT comparator and is followed by the conclusion of this paper.

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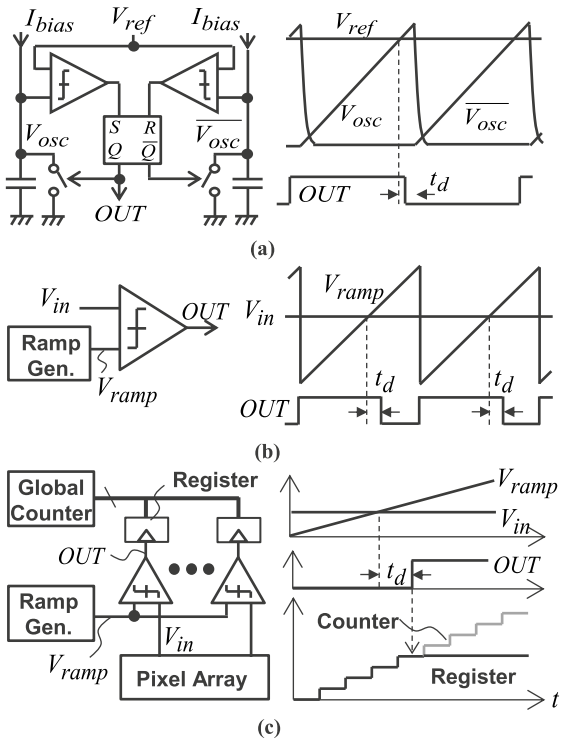

Fig. 1 Application of CT comparator; (a) relaxation oscillator, (b) pulse width modulator, (c) single-slope A/D converter.

2. Comparison of CT and DT Comparators

CT comparator has different function from discrete-time (DT) comparator. The former receives a differential input signal, and outputs a strobe ideally at the instance of zero-crossing of the input signal. The latter receives a strobe (or a clock edge) in addition to the input signal and outputs polarity of the input at the input strobe. It should be emphasized that the strobe is output in CT comparator whereas input in DT comparator.

Amplifiers are usually used in CT comparators whereas positive feedback circuits in DT comparators. An example of output waveform of the amplifier with step input is shown Fig. 2 (a). This waveform is expressed by a well-known formula shown in the figure: the output slew rate at $t = 0$ is $v_{in}g_m/\mathrm{C}$ and $v_{out}(\mathrm{t})$ asymptotes to the finite value $v_{in}g_m\mathrm{R}$. In the positive feedback circuit shown Fig. 2 (b), the voltage of the output port is initialized to the input voltage v_{in} and then positive feedback is formed right after the strobe. The output

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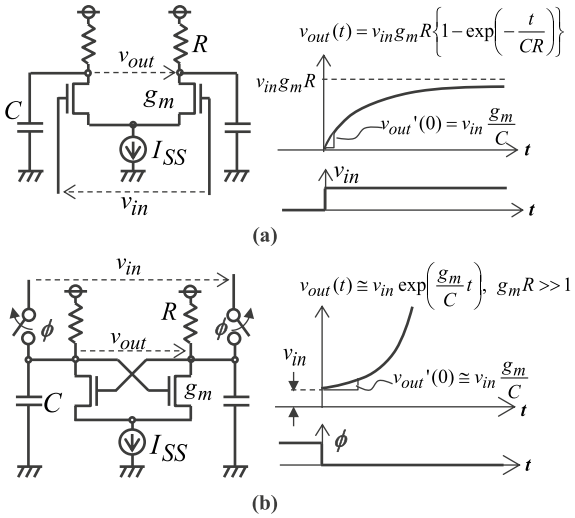

Fig. 2 Examples of output waveforms of (a) amplifier and (b) positive feedback.

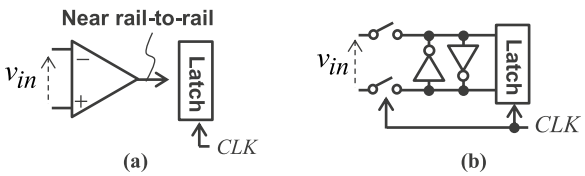

Fig. 3 DT comparator using (a) amplifier, (b) positive feedback.

waveform is obtained by a simple analysis and described in the figure assuming $g_m R \gg 1$. The output slew rate at t = 0 is identical to that in the amplifier, while the v_{out}(t) exponentially increases toward infinite. Therefore, the output of the positive feedback is faster and never caught up by that of the amplifier. Because of this advantage, the positive feedback is widely employed in DT comparators. On the other hand, CT comparators cannot utilize the positive feedback because of the lack of the input strobe, which is a serious constraint in designing CT comparators.

Note that it is possible and sometimes seen to design a DT comparator like Fig. 3 (a) where an amplifier amplifies the input to a near rail-to-rail signal. However, it is better to utilize the positive feedback as shown in Fig. 3 (b) because of the advantage discussed above. Especially dynamic comparators are the first candidates because they do not consume any static power. A dynamic comparator is analyzed in [4].

3. Investigation in Advance of Transient Analysis

Before the transient analysis, two examples of CT comparators are designed and simulated. The brock diagrams of these CT comparators are shown in Fig. 4 (a). Type A consists of a differential/single-ended signal converter (D/S) and a common-source inverter having a PMOS driver (PINV). Type B has a preamplifier (PA) at the frontend of them. Circuit diagrams of each block are shown in Fig. 4 (b). The PA is a wideband differential amplifier having resistive loads. The D/S acts as a high-gain amplifier if the input is small

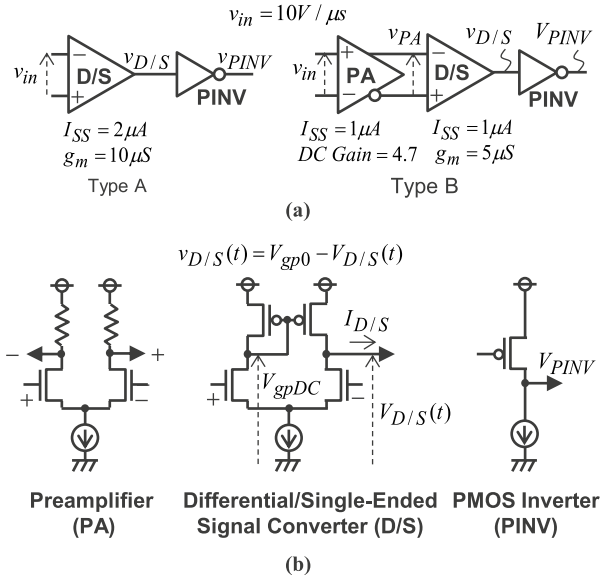

Fig. 4 Simulated CT comparators with and without preamplifier; (a) block diagram, (b) circuit configuration.

signal, while acts as a switched current source if the input is large enough to turn one of the differential pair completely on. The PINV follows the D/S to obtain a rail-to-rail output. The output voltage of the D/S $v_{D/S}$ is defined here as follows for the convenience of analysis:

$$v_{D/S}(t) \equiv V_{gpDC} - V_{D/S}(t), \tag{1}$$

where $V_{D/S}(t)$ is the node voltage (i.e., the voltage referenced to the ground) of the output and V_{gpDC} is the DC node voltage of the PMOS gate when the input voltage v_{in} is zero. Note that, in DC operation, $v_{D/S} = 0$ when $v_{in} = 0$ because $V_{D/S} = V_{gpDC}$.

Rising waveform is chosen as the polarity of the input ramp v_{in}. Because of this polarity, $V_{D/S}$ initially stays at V_{DD} and the PINV does not consume any current before its output starts rising. Moreover, the current consumption of the PINV after the output strobe can be minimized by disabling its bias current using this output strobe. It should also be noted, with this input polarity, the output voltage of the D/S defined by (1) is initially stays at the negative voltage V_{gspDC} ($\equiv V_{gpDC} - V_{DD}$) and is also rising waveform.

The total static currents in these CT comparators are designed to be the same. The key parameters are attached in Fig. 4 (a). It should be noted that these comparators can have systematic offset, which substantially shifts the timing of input zero-crossing. The input referred systematic offsets of these comparators is less than 15 μV.

The simulation result is shown in Fig. 5. In this simulation, each comparator is followed by 2 stages of CMOS inverter (not shown in Fig. 4). The output delay of Type B is 3.1 ns which is 240ps shorter than that of Type A though their current consumptions are the same. The reason is explained as follows: The slew rate of 10V/μsec generates 20mV input at t = 2nsec. Then the current from the D/S (see Fig. 4 (b)) is calculated as follows:

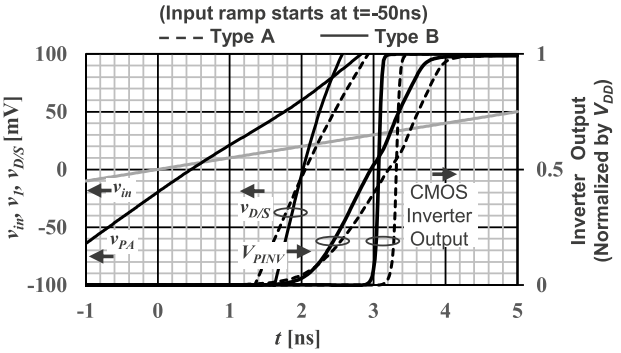

Fig. 5 Simulation result of CT comparators shown in Fig. 4.

$$\text{(Type A)} \quad I_{D/S} = 20mV \times 10\mu S = 200nA.$$
$$\text{(Type B)} \quad I_{D/S} = 20mV \times 4.7 \times 5\mu S = 470nA.$$

As shown here, because of *slew-rate amplification by preamplifier*, the delay of Type B is shorter despite that the transconductance of the D/S is reduced by half. Note that this calculation ignores the finite bandwidth of the PA. Therefore, next interest is the effect of the bandwidth on the comparator delay. It should also be noted that the current consumption of the PINV averaged from the beginning (−50ns) to the output strobe (including the two CMOS inverter delay) is less than 6% of the total current of the PA and the D/S. Therefore, the power consumption of the PINV can be made negligibly small by the technique described above.

4. Transient Analysis

Figure 6 shows a CT comparator with an n-stage PA. The input slew rate to the CT comparator is α and it is amplified stage by stage. This section derives an approximation formula that describes the total delay of the CT comparator.

4.1 Output Waveform of Amplifier

Each of the PA and the D/S shown in Fig. 4 (b) has the differential pair. Its differential output current i_{diff} is modeled as shown Fig. 7 (a), where v_{in} is the differential input voltage, I_{SS} is the tail current, and g_m is the transconductance of the differential pair when $v_{in} = 0$. In actual circuits, i_{diff} has non-linear dependence on v_{in} as shown by the dotted line. In this analysis, however, a PWL (piecewise linear) model shown by the solid line is employed for simplicity. Figure 7 (b) shows the equivalent circuit of the amplifier with a load capacitance C and a load resistance R. In actual circuits, they are modulated by non-linear dynamic effect. For example, the Miller capacitance contained in C depends on the output slew rate of the next stage and changes from moment to moment. However, it is assumed that they are constant and one of their terminals is grounded.

Figure 8 shows two examples of output waveforms. The black and gray lines are transient response (C > 0) and DC response (C = 0), respectively. Assuming v_{in} has the slew rate of α_{in} and crosses zero at $t = 0$, that is,

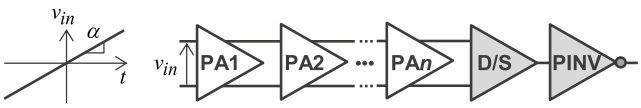

Fig. 6 Block diagram of CT comparator with multi-stage preamplifier.

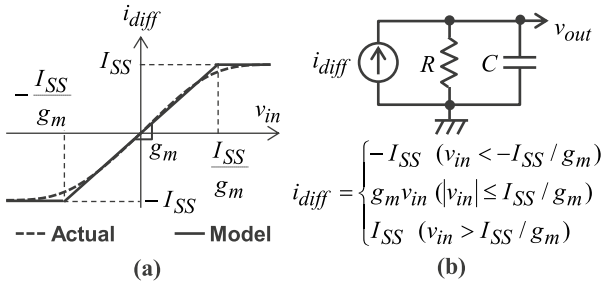

Fig. 7 Model of amplifier having differential pair; (a) PWL model for differential pair, (b) equivalent circuit of amplifier.

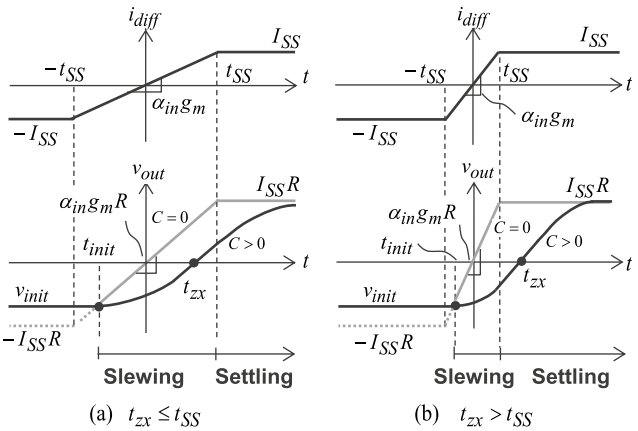

Fig. 8 Transient waveform of amplifier in two cases: output zero-crossing takes place before t_{SS} (a) and after t_{SS} (b).

$$v_{in}(t) = \alpha_{in} t, \tag{2}$$

the output current of the differential pair i_{diff} has slew rate of $\alpha_{in} g_m$ around $t = 0$ as shown in the upper side of Fig. 8. This current reaches I_{SS} at the slewing-settling boundary time t_{SS} which is given by,

$$t_{SS} = \frac{I_{SS}}{\alpha_{in} g_m}. \tag{3}$$

The lower side of Fig. 8 shows examples of output voltage waveform $v_{out}(t)$ which is defined as the difference of the instantaneous output voltage from its DC value when $v_{in} = 0$. The zero-crossing delay t_{zx} is the time output $v_{out}(t)$ crosses zero. This output zero crossing takes place in either slewing period (Fig. 8 (a)) or settling period (Fig. 8 (b)). The initial output voltage is denoted by v_{init}. It is always negative and defined by the output voltage at $t = -\infty$. If R is small and the differential pair always remains in saturation region, $v_{init} = -I_{SS}R$, which is the case in the PA. On the other hand, the initial voltage of the D/S is derived from (1) as,

$$v_{init}(D/S) = V_{gpDC} - V_{DD} \equiv V_{gspDC} < 0. \tag{4}$$

The output starts slewing at t_{init} which is given by,

$$t_{init} = \frac{v_{init}}{\alpha_{in} g_m R} \quad (-t_{SS} \le t_{init} < 0). \tag{5}$$

In the slewing period ($t_{init} < t \le t_{SS}$), $v_{out}(t)$ and its instantaneous slew rate $v_{out}'(t)$ are given by,

$$v_{out}(t) = \alpha g_m R\left\{t - CR + CR\exp\left(-\frac{t - t_{init}}{CR}\right)\right\}, \tag{6a}$$

$$v_{out}'(t) = \alpha_{in} g_m R\left\{1 - \exp\left(-\frac{t - t_{init}}{CR}\right)\right\}. \tag{6b}$$

Since the slew rate of the input voltage is given by $\alpha_{in}u(t - t_{init})$ where $u(t)$ is unit step function, (6b) can be obtained by replacing $v_{out}(t)$, v_{in}, and t in the equation in Fig. 2 (a) by $v_{out}'(t)$, α_{in} and $t - t_{init}$, respectively. The output $v_{out}(t)$ is then obtained by integrating (6b) from t_{init} to t. In the settling period ($t > t_{SS}$), $v_{out}(t)$ itself shows step response. Therefore, $v_{out}(t)$ and $v_{out}'(t)$ are given by,

$$v_{out}(t) = I_{SS}R - \{I_{SS}R - v_{out}(t_{SS})\}\exp\left(-\frac{t - t_{SS}}{CR}\right), \tag{7a}$$

$$v_{out}'(t) = \frac{1}{CR}\{I_{SS}R - v_{out}(t_{SS})\}\exp\left(-\frac{t - t_{SS}}{CR}\right), \tag{7b}$$

where $v_{out}(t_{SS})$ can be derived from (6a) and (3). Note that the output of the D/S can be clipped before it reaches $I_{SS}R$. This takes place when the right side of NMOS in the D/S in Fig. 4 (b) enters deep triode region. However, it is after the output zero-crossing t_{zx} and can be ignored in deriving t_{zx}.

4.2 Delay of Single-Stage Preamplifier

As mentioned in the previous subsection, the initial voltage of the PA is $-I_{SS}R$. Therefore, (5) is transformed using (3) into,

$$t_{init} = -t_{SS} = -\frac{I_{SS}}{\alpha_{in} g_m}, \tag{8}$$

If the output zero-crossing takes place in slewing period ($t_{zx} < t_{SS}$), the following relation is derived by replacing t_{init} by $-t_{SS}$ and setting $v_{out}(t_{zx}) = 0$ in (6a):

$$\frac{t_{zx}}{CR} = 1 - \exp\left(-\frac{t_{zx} + t_{SS}}{CR}\right). \tag{9}$$

The black solid line in Fig. 9 shows this relation. A numerical calculation is utilized here. This figure also shows the line $t_{zx} = t_{SS}$. As shown in the figure, $t_{zx} \le t_{SS}$ is satisfied when $t_{SS}/CR > 0.80$ ($\cong 1 - \exp(-2 \times 0.8)$), which is transformed using (3) into,

$$\alpha_{in} \le \frac{1.25}{g_m R} \cdot \frac{I_{SS}}{C}. \tag{10}$$

This is the condition that the output zero-crossing takes place in the slewing period as shown in Fig. 8 (a). Note that, since t_{SS} is inverse proportional to α_{in} as shown by (3), t_{SS}/CR in the latter stage of the PA is smaller than that in the earlier stage. As shown in the Fig. 9, the normalized output t_{zx}/CR slightly drops from 1 to 0.8 as t_{SS}/CR is decreased. However, this drop is ignored in the following analysis, and the following "constant delay approximation" is adopted:

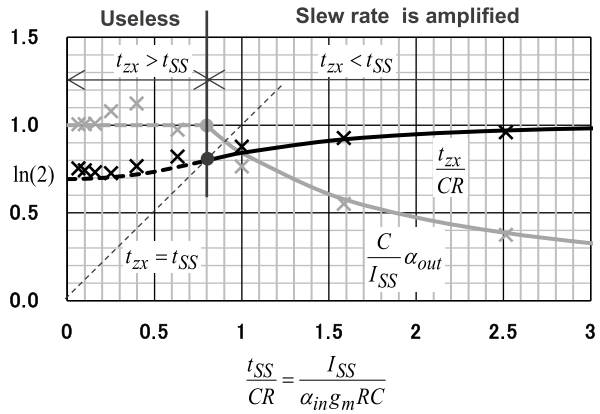

Fig. 9 Normalized output zero-crossing delay t_{zx}/CR of preamplifier and its normalized output slew rate $(C/I_{SS})\alpha_{out}$ as a function of t_{SS}/CR. "×" are results of SPICE simulation.

$$t_{zx} \cong CR \quad (t_{zx} \le t_{SS}). \tag{11}$$

The output slew rate at t_{zx} is derived from (6b), (8) and (3),

$$\alpha_{out} \equiv v_{out}'(t_{zx}) = \frac{I_{SS}}{C} \cdot \frac{t_{zx}}{t_{SS}} \quad (t_{zx} \le t_{SS}). \tag{12}$$

The gray solid line in Fig. 9 shows output slew rate normalized by I_{SS}/C. Since $t_{zx} \le t_{SS}$, the maximum slew rate is I_{SS}/C. From (11), (12) and (3) α_{out} is approximated as,

$$\alpha_{out} \cong g_m R\alpha_{in} \quad (t_{zx} \le t_{SS}). \tag{13}$$

which means the slew-rate gain and DC gain is identical. Results of SPICE simulation are also plotted in Fig. 9. In this plotting, g_m is extracted from DC operating point while R and C are calculated from DC gain and pole frequency in AC simulation. The results of analysis and simulation are well matched. In summary, if (10) is satisfied, the constant delay approximation can be adopted and the zero-crossing delay and the slew late can be approximated as (11) and (13), respectively.

If (10) is not satisfied, the output zero-crossing takes place in settling period (i.e., $t_{zx} > t_{SS}$) as shown in Fig. 8 (b). In this case, the output slew rate is derived by setting $v_{out}(t_{zx}) = 0$ in (7a) and combining it with $v_{out}'(t_{zx})$ given by (7b), which results in a constant value as follows:

$$\alpha_{out} \cong \frac{I_{SS}}{C} \quad (t_{zx} > t_{SS}). \tag{14}$$

This means that *the preamplifier which does not satisfies* (10) *does not amplify the slew rate.* Therefore, it only consumes power and is useless. For a reference, this saturated output slew rate is added to Fig. 9 (gray dotted line). The discontinuous derivative at the boundary comes from the PWL modeling shown in Fig. 7 (a). The normalized delay t_{zx}/CR in the case that $t_{zx} > t_{SS}$ is also shown by the

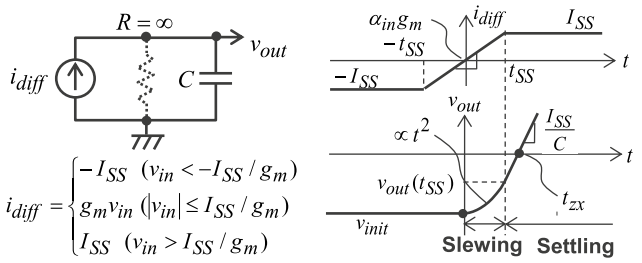

Fig. 10 Example of output waveform of D/S assuming $R = \infty$.

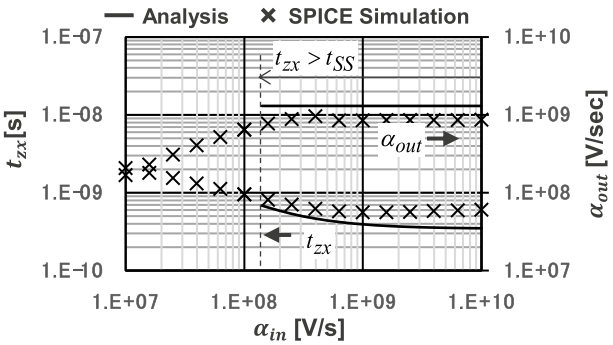

Fig. 11 Example of output zero-crossing delay t_{zx} and output slew rate α_{out} of D/S; I_{SS} = 1.0μA, g_m = 10mS, C = 0.77fF, v_{init} = −450mV.

black dotted line in Fig. 9. It is analytically derived by combining $v_{out}(t_{SS})$ given by (6a), (7a), and (8). If $\alpha_{in} = \infty$ ($t_{SS}/CR = 0$), the slewing period disappears and $v_{\rm out}$ shows step response with the finite time constant CR which starts rising at $t = 0$. In this case, $t_{zx} = CR\ln(2)$ where "ln(2)" comes from $v_{init} = -I_{SS}R$.

4.3 Delay of Differential/Single-Ended Signal Converter

In this subsection, the delay of the D/S is derived. Two assumption are introduced here. The first is that the load resistance R is infinite. The second is that, since the slew rate is amplified by the multi-stage PA, the input slew rate to the D/S is large enough for the output to cross zero in the settling period (i.e., $t_{zx} > t_{SS}$). An example of the output waveform is shown in Fig. 10. Because of the infinite load resistance, t_{init} given by (5) becomes zero and the D/S acts as an integrator. Since the current in the slewing period is $\alpha_{in}g_m t$, the output at t_{SS} is obtained by integrating the current from 0 to t_{SS} and combining it with (3) as,

$$v_{out}(t_{SS}) \cong v_{init} + \frac{1}{C}\int_0^{t_{SS}} \alpha_{in} g_m t dt = v_{init} + \frac{I_{SS}}{2C} t_{SS}, \quad (15)$$

where the initial voltage of the D/S v_{init} is given by (4). The second assumption $t_{zx} > t_{SS}$ is transformed into the following inequality by combining $v_{out}(t_{SS}) < 0$ in (15) with (3):

$$\alpha_{in} > \frac{{I_{SS}}^2}{2g_m C|v_{init}|}. \quad (16)$$

In the settling period, the current from the differential pair is I_{SS}. Therefore, $v_{out}(t)$ is obtained by integrating I_{SS} from t_{SS} to t and combining it with (15) as,

$$v_{out}(t) \cong v_{out}(t_{SS}) + \frac{1}{C}\int_{t_{SS}}^{t} I_{SS} dt = v_{init} + \frac{I_{SS}}{C}\left(t - \frac{t_{SS}}{2}\right). \quad (17)$$

The output zero-crossing delay is obtained by setting $v_{out}(t_{zx}) = 0$ in (17) and combining it with (3) as,

$$t_{zx} \cong \frac{1}{\alpha_{in}} \cdot \frac{I_{SS}}{2g_m} + \frac{C}{I_{SS}}|v_{init}| \quad (t_{zx} > t_{SS}). \quad (18)$$

Note that I_{SS2}/g_{m2} corresponds to V_{gs}-V_{th} of the differential pair in the D/S if it is biased in strong inversion and its typical value is 100~300mV. If it is biased in weak inversion, I_{SS2}/g_{m2} has the minimum of $2n_S k_B T/q$, where n_S is subthreshold factor and $2n_S k_B T/q$ is approximately 80mV at room temperature when $n_S = 1.5$. The output slew rate is directly obtained from (17) as,

$$\alpha_{out} \equiv {v_{out}}'(t_{zx}) \cong \frac{I_{SS}}{C} \quad (t_{zx} > t_{SS}), \quad (19)$$

which does not depend on input slew rate because $t_{zx} > t_{SS}$ (see the discussion on (14)).

Examples of t_{zx} given by (18) and α_{out} given by (19) under the condition given by (16) are plotted in Fig. 11 with results of SPICE simulation. The saturation of α_{out}, its boundary, and the shape of curve of t_{zx} (i.e., format of (18)) are reproduced well by the analysis. On the other hand, values of α_{out} and t_{zx} are overestimated and underestimated, respectively. However, the assumption of the infinite load resistance is retained in the following analysis to avoid complexity.

4.4 Total Delay of CT Comparator

In this subsection, total output zero-crossing delay of the CT comparator shown in Fig. 6 is derived. It is assumed here that the characteristics of each stage in the PA is identical. To distinguish the parameters of *each stage* of the PA, the D/S, and the PINV, suffixes of "1", "2", and "3" is added, respectively.

Under the constant delay approximation, the delay of the n-stage PA is given by nC_1R_1 while its output slew rate is given by $\alpha(g_{m1}R_1)^n$. Therefore, the total delay of the CT comparator is given by,

$$t_{zxtot} \cong t_{pd} + \frac{C_2}{I_{SS2}}|v_{init2}| + \frac{C_2}{I_{SS2}} \cdot \frac{I_{SS3}}{2g_{m3}} + \frac{C_3}{I_{SS3}}|v_{init3}|, \quad (20)$$

$$t_{pd} \equiv nC_1R_1 + \frac{1}{\alpha(g_{m1}R_1)^n} \cdot \frac{I_{SS2}}{2g_{m2}}, \quad (21)$$

where t_{pd} is the partial delay which depends on the PA design. The first term in (21) is the zero-crossing delay of the multi-stage PA and the second term corresponds to the delay required for the final output of the PA to rise from 0 to the voltage $I_{SS2}/(2g_{m2})$ (as for I_{SS2}/g_{m2} see the discussion on (18)). The zero-crossing delay of the D/S is given by

the sum of the second term in (21) and the second term in (20). The last two terms in (20) is the zero-crossing delay of the PINV. Since the load resistance of the PINV can also be approximated to infinite, the output zero-crossing delay is given by (18) where the input slew rate α_{in} is the output slew rate of the D/S given by (19). Note that $v_{init3} \cong -V_{DD}/2$.

5. Optimum Design of CT Comparator

5.1 Optimum Design of Multi-Stage Preamplifier

In this subsection, the condition for minimizing the partial delay defined by (24) is derived under the assumption that the total bias current of the PA is constant even when the number of stages n is changed. Figure 12 shows the method to keep the total bias current constant: dividing an original PA equally into n pieces while keeping the DC gain (= slew rate gain) *pre stage* $A_1 = g_{m1}R_1$ unchanged. This assumption makes A_1 independent of n and the minimum delay is derived from successive partial differentiation of (21) with A_1 and n. The other parameters are function of n and A_1. The parameter g_{m1} and R_1 is given by,

$$g_{m1} = \frac{g_{m1o}}{n}, \quad R_1 = \frac{A_1}{g_{m1}} = nR_{1o}, \tag{22}$$

where g_{m1o} and R_{1o} are the original transconductance and the load resistance before the division. The load capacitance consists of the gate capacitance of the next stage and parasitic capacitance of the load resistor inside the stage. After division, the former is $1/n$ times of the original values C_{G1o} and the latter is n times of the original value C_{R1o}. Therefore, C_1 can be modeled with proportional index p as follows:

$$C_1 = \frac{C_{G1o}}{n} + nC_{R1o} \cong n^p C_{1o}, \quad p = -1 \sim 1. \tag{23}$$

If the gate capacitance dominates the load capacitance, then $p = -1$, which is the case in the design of high-speed comparators. If the parasitic capacitance of the resistor dominates the load capacitance, then $p = 1$, which is the case in the design of slow but very low-power comparators. Equation (21) is transformed by combining it with (22) and (23) into,

$$t_{pd}(n, A_1) = \frac{n^{(p+2)}A_1}{\omega_{u1o}} + \frac{1}{\alpha {A_1}^n} \cdot \frac{I_{SS2}}{2g_{m2}}, \tag{24}$$

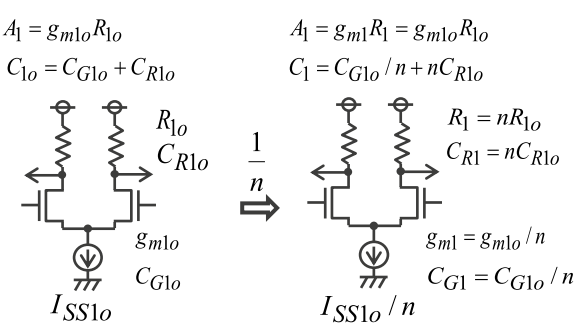

Fig. 12 Division of preamplifier to keep total bias current constant.

where ω_{u1o} is the unity frequency of the original PA before division and given by,

$$\omega_{u1o} \equiv \frac{g_{m1o}}{C_{1o}}. \tag{25}$$

The following relation is obtained by differentiating (24) with A_1 and setting it to zero:

$$\frac{1}{\alpha {A_{1opt}}^n} \cdot \frac{I_{SS2}}{2g_{m2}} = \frac{1}{n} \cdot \frac{n^{(p+2)}A_{1opt}}{\omega_{u1o}}, \tag{26}$$

where A_{1opt} is the optimum value of A_1 *before optimization of* n and therefore function of n. The right side of (26) is 1/n of the first term of (24) which corresponds to the delay per stage of PA. The left side of (26) is the second term of (24) and therefore it become identical with the delay per stage after A_1 is optimized. Equation (26) is transformed into,

$$A_{1opt} = \left\{ \frac{\omega_{u1o}}{n^{(p+1)}} \cdot \frac{I_{SS2}}{2\alpha g_{m2}} \right\}^{\frac{1}{n+1}}, \tag{27}$$

and the partial delay t_{pd} after optimization of A_1 is obtained by combining (24) and (27) as

$$t_{pd}(n, A_{1opt}) = (n+1)\left(\frac{I_{SS2}}{2\alpha g_{m2}}\right)^{\frac{1}{n+1}} \left\{ \frac{n^{(p+1)}}{\omega_{u1o}} \right\}^{\frac{n}{n+1}}. \tag{28}$$

Examples of the partial delay t_{pd} given by (28) is plotted in Fig. 13. Note that, higher slew rates α are employed for lower p in this plot. This is because p becomes lower in higher-speed comparator design (see the discussion on (23)) which usually receives the higher α. This figure shows that the optimum n is larger with lower p (i.e., in higher-speed comparator) or lower α.

Finally, the following relation is obtained by differentiating (28) with n and setting it to zero:

$$e^{(p+2)(n_{opt}+1)} \times {n_{opt}}^{(p+1)} = \frac{I_{SS2}}{2\alpha g_{m2}} \cdot \omega_{u1o}, \tag{29}$$

where n_{opt} is the optimum number of the PA stages after both A_1 and n are optimized. Figure 14 shows n_{opt} numerically calculated from (29). Note that if the gate capacitance of the next stage dominates the load capacitance, $p = -1$ and n_{opt} is analytically derived as,

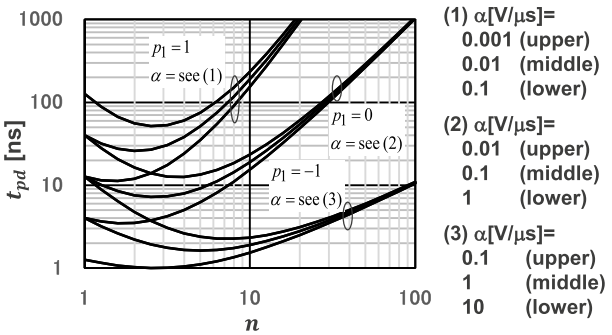

Fig. 13 Partial delay t_{pd} given by (27) or its equivalence (24) after optimization of DC gain of PA. (I_{SS2}/g_{m2} = 80mV, ω_{uo} = 10Grad/s)

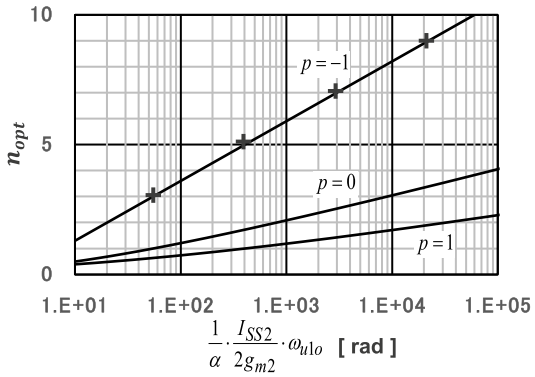

Fig. 14 Optimum number of stages of PA calculated from (34). Design parameters used for the SPICE simulation is shown by "+".

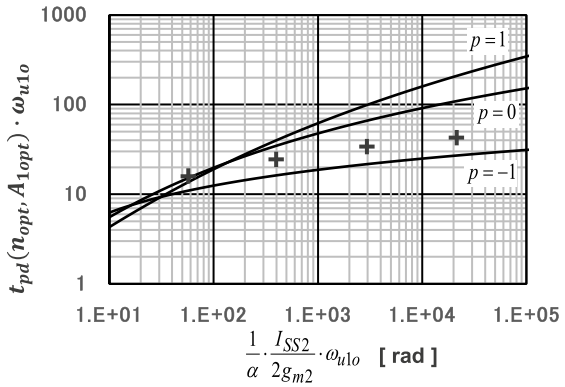

Fig. 15 Minimum partial delay t_{pd} calculated from (35) (normalized by C_{1or}/g_{m1or}). SPICE simulation results when $p = -1$ are shown by "+".

$$n_{opt} = \ln\left(\frac{I_{SS2}}{2\alpha g_{m2}}\omega_{u1o}\right) - 1. \tag{30}$$

The optimum DC gain after optimization of n can be calculated from (27) and (29) and it is given by the following simple formula:

$$A_{opt}\Big|_{n=n_{opt}} = e^{p+2}. \tag{31}$$

Therefore, the optimum DC gain per stage is determined by only the proportional index p which depends on the elements dominating the load capacitance in the PA as described in the discussion on (23). Note that, when $p = 1$ (in the case that the parasitic capacitance of the load resistor dominates the load capacitance), the optimum DC gain is $e^3 \cong 20$ which may require a common-mode feedback (CMFB) in the amplifier. To suppress the power required for the CMFB is left for the future study. The minimum partial delay after optimization of A_1 and n is obtained by combining (28) and (29) as,

$$t_{pd}(n_{opt}, A_{1opt}) = \frac{n_{opt}+1}{e^{n_{opt}(p+2)}}\cdot\frac{I_{SS2}}{2\alpha g_{m2}}. \tag{32}$$

As shown in (32), smaller I_{SS2}/g_{m2} gives shorter partial delay. However, remember that I_{SS2}/g_{m2} has a lower limit of $2n_S k_B T/q$ as described in the discussion on (18). The minimum partial delay normalized by $1/\omega_{u1o}$ is shown in Fig. 15. Note that it depends on ω_{u1o} (the unity gain frequency of the PA before the division) because n_{opt} depends on ω_{u1o}. It also should be noted that the gradient of the curve shown in Fig. 15 is less than 1. This means larger ω_{u1o} gives shorter t_{pd}. The optimum design of the PA can be estimated using Figs. 14 and 15. For example, assuming,

$$\alpha = 1\text{V}/\mu\text{s}, I_{SS2}/g_{m2} = 80\text{mV}, \text{and } \omega_{uo} = 10\text{Grad/s}, p = -1$$

the value of X axis in Figs. 14 and 15 is 400 rad. Therefore,

$$n_{opt} = 5,\ t_{pd} = 1.6\text{ns}\ (t_{pd}\omega_{uo} = 16)$$

is read from Fig. 14 and 15, respectively. The "+" in the Figs. 14 and 15 is SPICE simulation result in the case $p = -1$ (in the case that the gate capacitance of the next stage dominates the load capacitance). In these simulation, the input slew rate α is selected so that the partial delay t_{pd} is not affected by rounding of n_{opt}. Except that the analysis underestimates the partial delay approximately by $-30\sim-35\%$, the results of the analysis and simulation are matched well.

Remember that the stage in the PA which does not satisfy (10) does not amplify its input slew rate and is useless. The last stage of the PA is examined here because it receives highest input slew rate. Using the optimized DC gain per stage given by (31) and the relation of I_{SS1} and C_1 with their original values defined in Fig. 12, (10) is transformed into,

$$\alpha e^{(p+2)n_{opt}} \times {n_{opt}}^{p+1} \le 1.25\cdot\frac{I_{SS1o}}{C_{1o}}, \tag{33}$$

which is further transformed by being combined with (29) into,

$$\frac{I_{SS1o}/g_{m1o}}{I_{SS2}/g_{m2}} \ge \frac{1}{2.5e^{(p+2)}} = 0.02 \sim 0.15. \tag{34}$$

For example, if the I_{SS}/g_m of the PA and the D/S are designed to be the same, (34) is satisfied with a large margin. As shown in this calculation, all stages of the PA after the optimization of the number of stages and DC gain amplifies the slew rate.

5.2 Design of Differential/Single-Ended Signal Converter and Common-Source Inverter

The total delay of the CT comparator given by (20) is transformed using the partial delay after optimization of preamplifier given by (32) into,

$$t_{zxtot} \cong \frac{n_{opt}+1}{e^{n_{opt}(p+2)}}\cdot\frac{I_{SS2}}{2\alpha g_{m2}} + \frac{C_2}{I_{SS2}}|v_{init2}| + \frac{C_2}{I_{SS2}}\cdot\frac{I_{SS3}}{2g_{m3}} + \frac{C_3}{I_{SS3}}|v_{init3}|. \tag{35}$$

The first two terms correspond to sum of the delays of the multi-stage PA and the D/S. The last two terms correspond to the delay of the PINV. Note that *to increase I_{SS} does not always result in shorter delay*. As already described in the discussion on (32), the first term become shortest if I_{SS2}/g_{m2}

is at its lower limit of $2n_S k_B T/q$. Therefore, biasing the differential pair on the boundary of strong and weak inversions is the first candidate in the design of the D/S. However, if this biasing makes the second term (the time required to charge C_2 from v_{init} to 0) larger than the first term, more I_{SS2} can results in shorter total delay.

To avoid complex calculations, two approximations are introduced here. The first is that n_{opt} in the first term in (35) is treated as a constant because its dependence on I_{SS2} is weak (approximately logarithmic) as shown in Fig. 14. The second is that the third term in (35) is ignored when optimizing I_{SS2}. This makes the optimization of I_{SS2} independent of I_{SS3}. Under these approximations, (35) behaves as $f(x) = ax + b/x$ where a and b are coefficients, and x corresponds to I_{SS2} or I_{SS3}. This function $f(x)$ has a minimum value of $2\sqrt{ab}$ when $x = \sqrt{b/a}$ (or $ax = b/x$). Therefore, I_{SS2} which realizes the minimum delay of the first and second terms is given by,

$$I_{SS2opt} \approx \sqrt{\alpha \frac{e^{n_{opt}(p+2)}}{n_{opt}+1} \cdot 2g_{m2}C_2|v_{init2}|}. \tag{36}$$

If this value is larger than $2g_{m2}n_S k_B T/q$, there is a chance to shorten the total delay more by increasing I_{SS2}. Similarly, I_{SS3} which realizes the minimum delay of third and fourth terms is given by,

$$I_{SS3opt} \approx \sqrt{\frac{I_{SS2opt}}{C_2} \cdot 2\alpha g_{m3}C_3|v_{init3}|}. \tag{37}$$

Remember that static current of the PINV can be made zero by the dynamic operation described in Sect. 3. Therefore, setting I_{SS3} to the value given by (37) does not impact on the total power consumption.

6. Conclusion

This paper analyzes the CT comparator having the multi-stage preamplifier with the differential/single-end signal converter and the common-source inverter in the back-end. The constant delay approximation is introduced in the preamplifier modeling while clarifying the boundary beyond which the preamplifier does not amplify the input slew rate. Both the differential/single-end signal converter and the common-source inverter are modeled as integrators for simplicity. The multi-stage preamplifier is optimized with keeping power consumption constant. The results include that the optimum DC gain per stage is e if the gate capacitance of the next stage dominates the load capacitance while e^3 if the parasitic capacitance of the load resistor inside the stage dominates. The optimum number of stage becomes larger as input slew rate becomes smaller or as the gate capacitance dominates more. This paper also discusses the optimum design of the differential/single-end signal converter and the common-source inverter. The delay model derived in this paper and the results of the optimization as well as other design tips suggested in this paper are helpful in designing CT comparators.

References

[1] K. Choe, O.D. Bernal, D. Nuttman, and M. Je, "A Precision Relaxation Oscillator with a Self-Clocked Offset-Cancellation Scheme for Implantable Biomedical SoCs," IEEE International Solid-State Circuits Conference Dig. Tech. Pap., pp.402–403, 2009.

[2] T.Y. Man, P.K.T. Mok, and M.J. Chan, "A 0.9-V Input Discontinuous-Condition-Mode Boost Converter With CMOS-Control Rectifier," IEEE J. Solid-State Circuits, vol.43, no.9, pp.2036–2046, 2008.

[3] S. Okura, O. Nishikido, Y. Sadanaga, Y. Kosaka, N. Araki, K. Ueda, and F. Morishita, "A 3.7 M-Pixel 1300-fps CMOS Image Sensor With 5.0 G-Pixel/s High-Speed Readout Circuit," IEEE J. Solid-State Circuits, vol.50, no.4, pp.1016–1024, 2015.

[4] H. Xu and A.A. Abidi, "Analysis and Design of Regenerative Comparators for Low Offset and Noise," IEEE Trans. Circuits Syst. I, Reg. Papers, vol.66, no.8. pp.2817–2830, 2019.

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