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Flexoelectric Effect on Image Sticking Caused by Residual Direct Current Voltage and Flicker Phenomenon in Fringe-Field Switching Mode Liquid Crystal Display

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SUMMARY Although transmittance changes like a quadratic function due to the DC offset voltage in FFS mode LCD, its bottom position and flicker minimum DC offset voltage varies depending on the gray level due to the flexoelectric effect. We demonstrated how the influence of the flexoelectric effect changes depending on the electrode width or black matrix position.

key words: *FFS, image sticking, flicker, flexoelectric effect*

1. Introduction

Good image quality is provided by both in-plane switching (IPS) mode liquid crystal displays (LCDs) [1] and fringe-field switching (FFS) mode LCDs [2], which are derived from IPS mode LCDs. However, FFS mode LCDs are superior to IPS mode LCDs in terms of low driving voltage and fast response time because it is possible to use small dielectric anisotropy ($\Delta\varepsilon$) liquid crystal (LC) materials with low viscosity in FFS mode LCDs due to their strong electric field near the substrate with slit electrodes. For this reason, FFS mode LCDs have been widely used for various applications, such as mobile phones, tablets, monitors, televisions and in-vehicle displays. However, the FFS mode is more susceptible to the image-sticking problem than the other modes. Furthermore, there is a flicker shift problem which is often occurred in FFS mode LCDs.

As shown in Fig. 1, generally, image sticking can be estimated by displaying a checkerboard pattern for a specified time and then a solid pattern with various gray levels. Although several causes of image-sticking in LCDs are well known [3], we believe the most important cause is residual DC (RDC) voltage.

As shown in Fig. 2, transmittance at low or middle gray level changes like a quadratic function when a DC offset voltage is applied. This quadratic relationship between DC offset and transmittance is called D–T property in this paper. Although LCDs are driven by AC voltage, the term of transmittance means averaged transmittance of positive and negative frames. When a DC offset voltage is applied, the positive and negative voltages applied to the LC layer become asymmetric. Similarly, as these voltages become asymmetric, the bottom of the D–T property shifts horizontally when the RDC voltage is generated. Therefore, if the amounts of the RDC voltage become different between adjacent black and white patterns, the boundary between them becomes visible. This is the image-sticking problem caused by the RDC voltage [3].

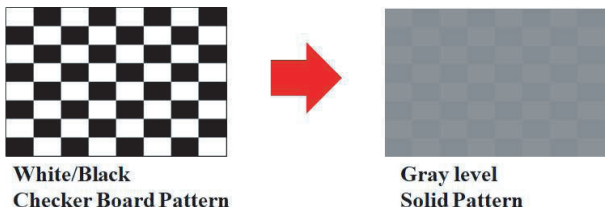

Fig. 1 Estimating degree of image sticking

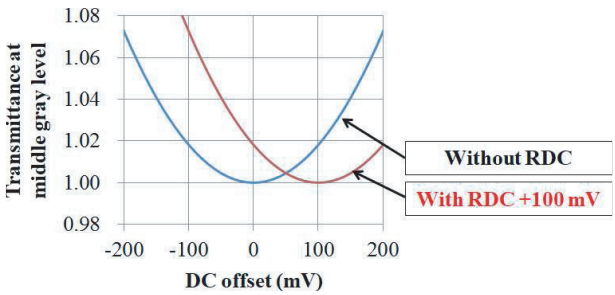

Fig. 2 D–T property with and without RDC voltage

Flicker shift is a phenomenon in which the flicker minimum common electrode voltage (Vcom) changes with time and saturates after adjusting Vcom to minimize the flicker value. Although there are several flicker shift phenomenon factors in FFS mode LCDs [4]–[6], one of the important factors is the flexoelectric effect [7]. Although the LCD is generally driven by a refresh rate of 60 Hz, a 30 Hz flicker component is generated, when the voltage applied between the pixel and common electrodes becomes asymmetric. When Vcom is adjusted to minimize the flicker value, the voltage applied between their electrodes becomes symmetric in other LCD modes, such as twist nematic (TN) or vertical alignment (VA). However, the DC offset voltage is applied between the pixel and common electrodes in FFS mode, if similar adjusting of Vcom is done in TN or VA mode, because the flexoelectric effect generates a 30 Hz flicker due to

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changing transmittances between the positive and negative frames [8]. Thus, to suppress the flicker shift phenomenon in FFS mode, it is important to distinguish the divide flicker factors due to the flexoelectric effect from the other ones.

In this paper, we discuss both image-sticking caused by RDC voltage and flicker caused by flexoelectric effect. Although the shape (width or bottom position) of the D–T property is important to understand image sticking, we found that the flexoelectric effect affects not only flicker but also the D–T property bottom position, and both have gray level dependence. We simulate their gray level dependence by changing the cell parameters such as the slit electrode width and black matrix (BM) width in FFS mode LCDs. Furthermore, we measured the D–T property and flicker minimum DC offset voltage of the LCD panel and compared them with the simulation results.

2. Measurement and Simulation

2.1 Method of Measuring D–T Property and Flicker Minimum DC Offset Voltage for Each Gray Level

We measured D–T properties and flicker minimum DC offset voltages at 32 Gray, 64 Gray and 128 Gray. The LCD panel was driven by static driving, which applies DC +20 V to the gate line. The gate was always open and driven by square waves produced by a function generator. Static driving is an AC driving method that is free from the effect of feed-through voltages because the gate voltage is constant during measurement.

First, we measured the voltage–transmittance (V–T) property to calculate each of the gray level voltages, as shown in Table 1. We defined the zero gray level as black and the 255 gray level as white, and calculated each gray level to have gamma value of 2.2.

For the D–T property measurement, we measured the transmittance when applying a DC offset voltage (−0.2, 0, +0.2 V) at each gray level, and we calculated the D–T property and its bottom position by fitting the transmittance of three points to quadratic function.

Then, for the flicker minimum DC offset voltage, we measured the flicker value using color analyzer CA-410 made by Konica Minolta and found the flicker minimum DC offset voltage. It is possible to generate the RDC voltage between the pixel and common electrodes during measurement of the D–T property and flicker minimum DC offset voltage because the DC voltage is applied for a short time. We always keep applying AC 0.01 V without the DC voltage between the pixel and common electrodes before we measure one point of data such as transmittance and flicker.

Table 1 Measurement results for each gray level voltage

Gray level	Voltage
32 Gray	1.6 V
64 Gray	2.1 V
128 Gray	2.7 V
255 Gray	5.8 V

Then, we check the flicker minimum DC offset voltage at the 128 Gray level before and after the measurement and confirm that an RDC voltage is not generated.

2.2 Simulation Method of D–T Property and Flicker Minimum DC Offset Voltage

We simulated the D–T property in the FFS cell shown in Fig. 3 using the cell and LC parameter shown in Tables 2 and 3, respectively. First, we simulated the V–T property to calculate each of the gray level voltages, as shown in Table 4. This simulation does not consider the flexoelectric effect.

Next, we executed a D–T property simulation at each gray level using the two methods. In the first conventional method, we calculated the D–T property using the V–T property from −7 V to +7 V, as shown in Fig. 4. When we calculated the D–T property at AC 2.0 V, for example, the

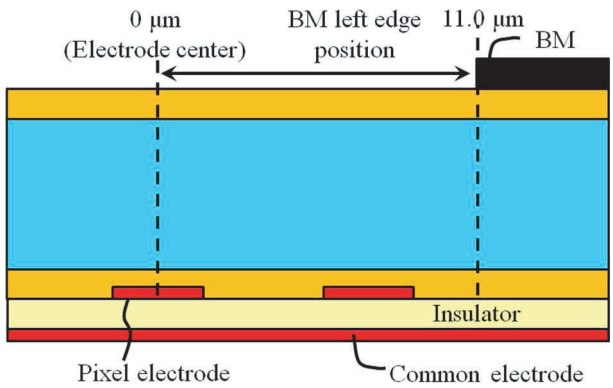

Fig. 3 Simulation model of FFS cell.

Table 2 Cell parameters of FFS cell

Insulator	Thickness	300 nm	
	ε	6.0	
Pixel electrode	Pitch	7.0 μm	
	Width	2.6 μm	3.0 μm
	Space	4.4 μm	4.0 μm
Alignment layer	Thickness	100 nm	
	ε	3.3	
BM left edge position		0 –– 11 μm	
Slit angle (LC director)		7 deg.	

Table 3 LC parameters

ε parallel	7.4
ε perpendicular	2.8
K11	14.2 pN
K22	7.1 pN
K33	16.0 pN
γ_1	61 mPa·s

Table 4 Simulation results for each gray level voltage without flexoelectric effect

Gray level	Voltage
32 Gray	1.6 V
64 Gray	2.0 V
128 Gray	2.6 V
255 Gray	5.5 V

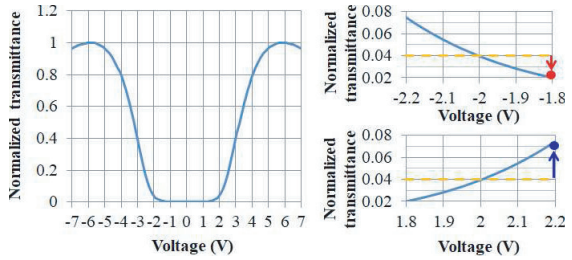

Fig. 4 D–T property simulation method (Static method)

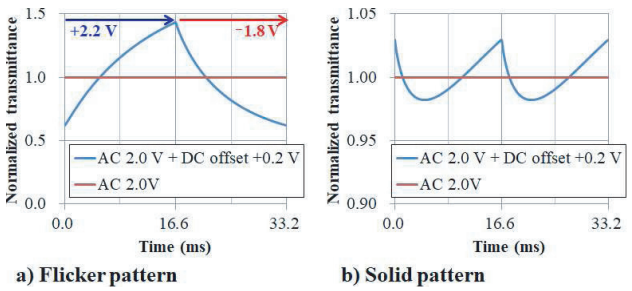

Fig. 5 D–T property simulation method (Dynamic method)

transmittance with DC offset voltage +0.2 V was calculated by averaging the transmittances at +2.2 V and −1.8 V. The transmittance with DC offset +0.2 V is higher than that without a DC offset because the transmittance rising ratio at +2.2 V is larger than that of the falling ratio at −1.8 V, as shown in Fig. 4. Similarly, we calculated the transmittance at AC 2.0 V with DC offset 0 V and −0.2 V, and then we calculated the D–T property by fitting the transmittance of three points to a quadratic function.

The simulation of the V–T property was carried out using the static analysis mode of LCD Master 2D made by Shintech, Inc. ("static method"). In this method, LC directors are saturated against the applied DC voltage.

In the second method, which we propose, we calculated to average the transmittance of each frame of positive and negative after the waveform of transmittance stabilized. The resulting waveform of transmittance is shown in Fig. 5 a). The waveform thus obtained corresponds to that of the flicker pattern display only for the positive pixels in the first frame and negative pixels in the second frame. When we estimate the image sticking of LCD, we actually see both positive and negative pixels at the same time. For this reason, the waveform became shaped as shown in Fig. 5 b), and the averaged transmittance becomes larger than when the DC offset is not applied. This simulation was carried out using dynamic analysis mode of LCD Master 2 D ("Dynamic method"). We calculated the D–T property using a quadratic function fitting like a static method.

Furthermore, we executed the flicker minimum DC offset voltage simulation using the dynamic method. When we executed the LCDMaster 2D simulations mentioned above, the flexoelectric effect was not considered. However, the flexoelectric effect was added to the LCD Master 2D in the next formula, and we can simulate the flexoelectric effect.

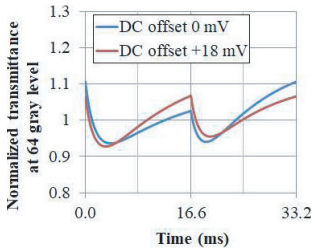

Fig. 6 Results for flicker minimum waveform simulation

$$\boldsymbol{P}_f = e_s \cdot \boldsymbol{n}(\nabla \cdot \boldsymbol{n}) + e_b \cdot \boldsymbol{n} \times (\nabla \times \boldsymbol{n})$$

$\boldsymbol{P}_f$: Flexoelectric polarization

e_s and e_b: Splay and bend flexoelectric LC coefficients

$\boldsymbol{n}$: Vector description of the LC director

And we used the flexoelectric coefficient of e_s and e_b as +10 pC/m, respectively.

When transmittance difference between positive and negative frames occurs due to the flexoelectric effect, a 30 Hz flicker component is generated, as shown in Fig. 6. We find the flicker minimum DC offset voltage at each gray level to repeat the simulation changing the DC offset voltage until we obtain the flicker minimum transmittance waveform.

3. Results and Discussion

3.1 D–T Property Measurement Results for Each Gray Level

We measured the D–T property of the LCD panels driven by static driving. The measurement results for each gray level are shown in Fig. 7. The transmittance changing ratio against the DC offset voltage (D–T property width) at 32 Gray and 64 Gray (low gray level) are larger than that at 128 Gray (middle gray level). Furthermore, the bottom position of the D–T property varies depending on gray level. We studied why the D–T property width and bottom position vary depending on the gray level by simulation.

As mentioned above, when the transmittance of gray level changes due to the DC offset voltage, how much DC offset is generated, and does the image sticking problem occur? We focused on the JND (just noticeable difference) of brightness to calculate the acceptable DC offset voltages when image sticking occurs at each gray level [9]. The JND of brightness based on the GSDF (Grayscale Standard of Display Function) of DICOM (Digital Imaging and Communications in Medicine) standard, which is the medical monitor standard, is shown in Fig. 8 [10]. This means that it can be recognized that there is a difference of brightness, for example, if there is a difference of about 26 cd/m^2 (0.65%) at 4000 cd/m^2 of the highest luminance. Although the JND of brightness becomes smaller as the luminance becomes darker, as shown in Fig. 8 a), the JND ratio to luminance increases as the luminance becomes darker, as shown in Fig. 8 b).

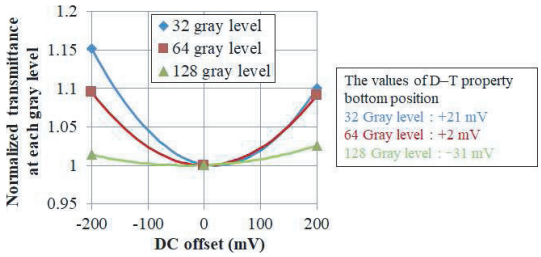

Fig. 7 Measurement results of D–T property

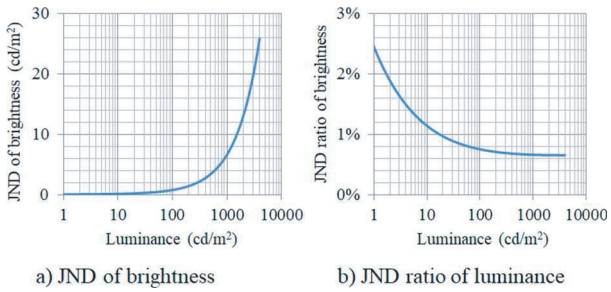

Fig. 8 JND (Just Noticeable Difference) of brightness

Table 5 Measurement results of DC offset voltage giving JND

Gray level		32	64	128	255
Normalized transmittance		0.1040	0.0478	0.2195	1.0000
L [cd/m^2]		5.20	23.89	109.76	500.00
JND [%]		1.37	0.93	0.74	-
D-T property bottom position [mV]		+21	+2	−31	-
DC offset voltage giving JND [mV]	Range	139	126	255	-
	Plus	+90	+65	+97	-
	Minus	−49	−61	−158	-

The JND ratio of luminance and DC offset voltage giving the JND are shown in Table 5. We defined white luminance as 500 cd/m^2, and calculated the luminance at each gray level. Next, we calculated the JND at each gray level using the data shown in Fig. 8. Finally, we calculated the DC offset voltage giving JND using the JND value and D–T property for each gray level.

Although the JND value at 32 Gray level is bigger than that at 64 Gray level, the range of DC offset voltage giving the JND is similar. We think the effect of the JND difference cancels the effect of the D–T property width. Although JND value is similar at 64 and 128 Gray levels, the range of the DC offset voltage giving the JND at 64 Gray level is twice that of the 128 Gray level. The difference clearly depends on the D–T property width.

3.2 Flicker Minimum DC Offset Voltage and D–T Property Bottom Position Measurement Results for Each Gray Level

We measured the flicker minimum DC offset voltage for each gray level. The measurement results of the flicker minimum DC offset voltage and D–T property bottom position are shown in Fig. 9. Although both DC offset values decrease as increasing of Gray level, their values do not have

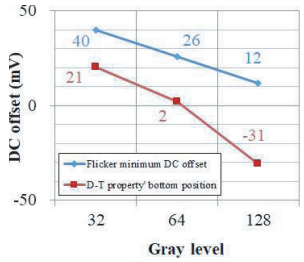

Fig. 9 Measurement results of flicker minimum DC voltage and D–T property bottom position

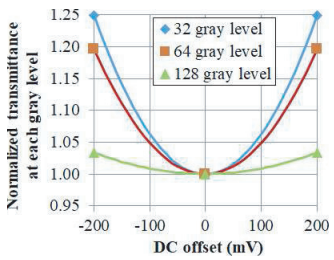

Fig. 10 D–T property simulation results at each gray level (static method)

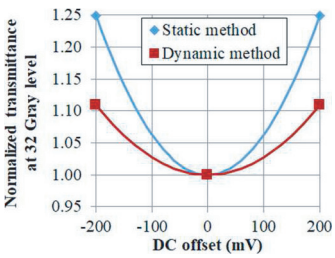

Fig. 11 D–T property simulation results at 32 Gray level

same value at each gray level. We studied why both properties varied depending on the gray level by simulation, too.

3.3 D–T Property Simulation Results for Each Gray Level Without Flexoelectric Effect by Static Method

The D–T property simulation results obtained by static method are shown in Fig. 10. In this section, we simulated under the following conditions; electrode width w of 2.6 μm and BM position of 11 μm.

Although the D–T property width is narrowest at 32 Gray level and widest at 128 Gray level, those are same in our measurement results shown in Fig. 7. As the static method uses V–T property to calculate D–T property, we consider that the D–T property width is related to the average rate of change on V–T property. In other words, the average rate of change on V–T property at 32 Gray level is larger than that at 128 Gray level.

Then we compared the D–T properties obtained by the static method and dynamic method at a refresh rate of 60 Hz. The simulation results are shown in Figs. 11 to 13. Although the D–T property width by static method is small compared with that of the dynamic method in each figure, we believe

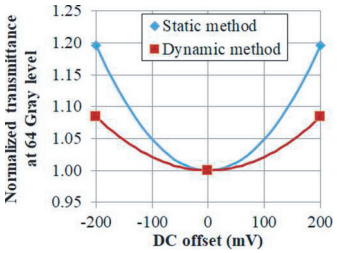

Fig. 12 D–T property simulation results at 64 Gray level

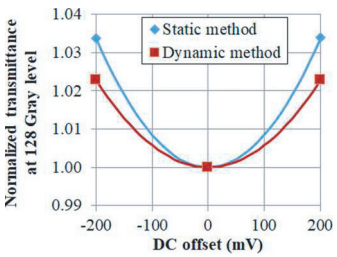

Fig. 13 D–T property simulation results at 128 Gray level

Table 6 Simulation results of DC offset voltage giving JND

Gray level		32	64	128
JND [%]		1.37	0.93	0.74
DC offset voltage giving JND [mV]	Static method	±47	±44	±93
	Dynamic method	±72	±67	±114

liquid crystal does not sufficiently respond at a refresh rate frequency of 60 Hz. Furthermore, the difference of the D–T properties width between the static method and dynamic method at 128 Gray level is smaller than that at 32 Gray level. We think the reason is the differences between the LC response times at 128 Gray level and at 32 Gray level. Because the response time at 128 Gray level is faster than that at 32 Gray level, the difference between the static method and dynamic method is small at 128 Gray level.

If the LC response time becomes faster, transmittance at 128 Gray level due to DC offset voltage increases, so that the image sticking caused by RDC voltage will be deteriorated because D–T property is closer to that of static method.

Thus, the D–T property is defined by not only the average rate of change on the V–T property but also the LC response property. In other word, image sticking due to the RDC voltage may become worse when the LC response is fast.

The JND values and calculated DC offset voltages giving the JND are shown in Table 6. Although the range of DC offset voltages giving the JND at 128 Gray level is twice those at low gray levels by static method, it at 128 Gray level is not twice those at low gray levels by dynamic method.

3.4 D–T Property Simulation Results for Each Gray Level with Flexoelectric Effect by Dynamic Method

We executed the D–T property and flicker minimum DC offset voltage simulations by dynamic method considering the flexoelectric effect under the following conditions; electrode

Table 7 Simulation results for each gray level voltage with and w/o flexoelectric effect

Gray level	Voltage	
	with flexoelectric effect	w/o flexoelectric effect
32 Gray	1.5 V	1.6 V
64 Gray	1.9 V	2.0 V
128 Gray	2.5 V	2.6 V
255 Gray	5.3 V	5.5 V

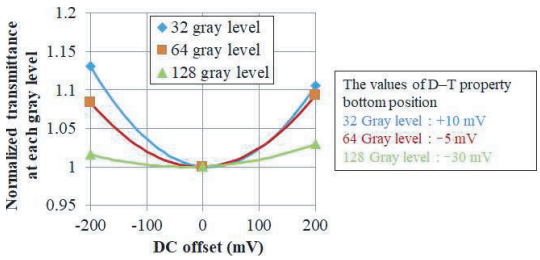

Fig. 14 D–T property simulation results at each gray level with flexoelectric effect (dynamic method); w = 2.6 μm, BM left edge position = 11 μm

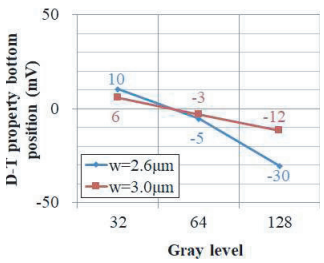

Fig. 15 Simulation results for gray level dependence of D–T property bottom position (dynamic method); BM left edge position = 11 μm

width w of 2.6 μm and BM left edge position of 11 μm. First, we simulated the V–T property to calculate each of the gray level voltages, as shown in Table 7.

The simulation results of V–T property without flexoelectric effect are shown in Table 7, too. When the flexoelectric effect exits, the V–T property slightly shifts to low voltage because it affects the dielectric anisotropy of the LC layer a little bit large, locally.

Next, we simulated the D–T property with different electrode width. Although the simulation results at electrode width w = 2.6 μm are shown in Fig. 14, the D–T property bottom positions varied depending on the gray level like the measurement results shown in Fig. 7.

Furthermore, we simulated the D–T property bottom position and flicker minimum DC offset voltage by varying the electrode width. As shown in Figs. 15 and 16, respectively, dependence against gray level changes due to change of the electrode width, and the dependence at electrode width w = 3.0 μm is smaller than that at electrode width w = 2.6 μm.

Furthermore, we simulated the D–T property bottom position and flicker minimum DC offset voltage varying the BM left edge position to understand why their gray level dependencies change depending on electrode width. The

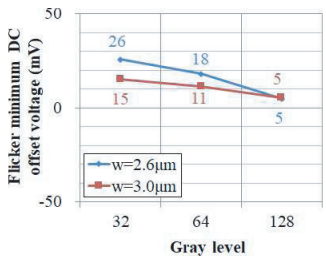

Fig. 16 Simulation results for gray level dependence of flicker minimum DC offset voltage (dynamic method); BM left edge position = 11 μm

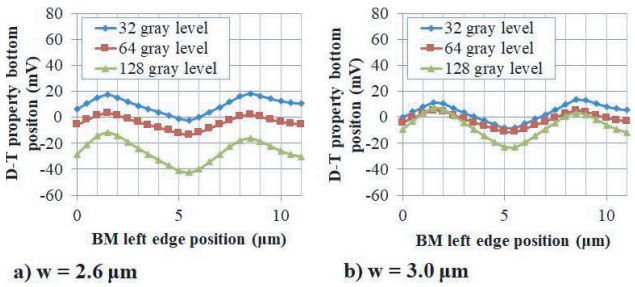

Fig. 17 Simulation results of D–T property bottom position varying BM left edge position (dynamic method)

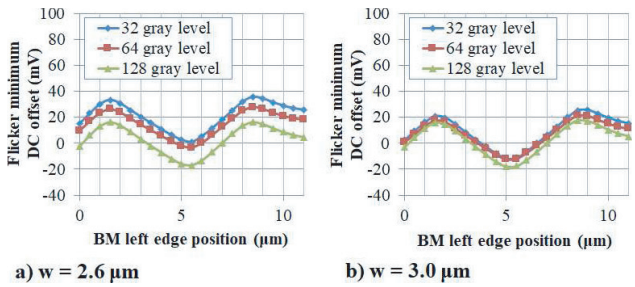

Fig. 18 Simulation results of flicker minimum DC offset voltage varying BM left edge position (dynamic method)

BM left edge position changes 11 μm, which matches our LCD panel using measurement, to 0 μm, which is the center of the electrode. As shown in Fig. 17, the D–T property bottom positions of each gray level fluctuate at a 7 μm period of the BM left edge position, which is coincident with the electrode pitch. Similarly, the flicker minimum DC offset voltage of each gray level also fluctuates at a 7 μm period of the BM left edge position, as shown in Fig. 18. Both of D–T property bottom position and flicker minimum DC offset voltage for each gray level almost correspond at w = 3.0 μm, but do not correspond at w = 2.6 μm.

The transmittance profile simulation results at 128 Gray level are shown in Fig. 19. The transmittance of the positive frame at the electrode center and negative frame at the slit center falls, and that of the opposite frame at each position rises due to the flexoelectric effect. In the case of w = 3.0 μm (lower image in Fig. 19), the transmittance profile of a positive (or negative) frame at the electrode center is similar to that of the negative (or positive) frame at the slit center, but in the case of w = 2.6 μm (upper image in

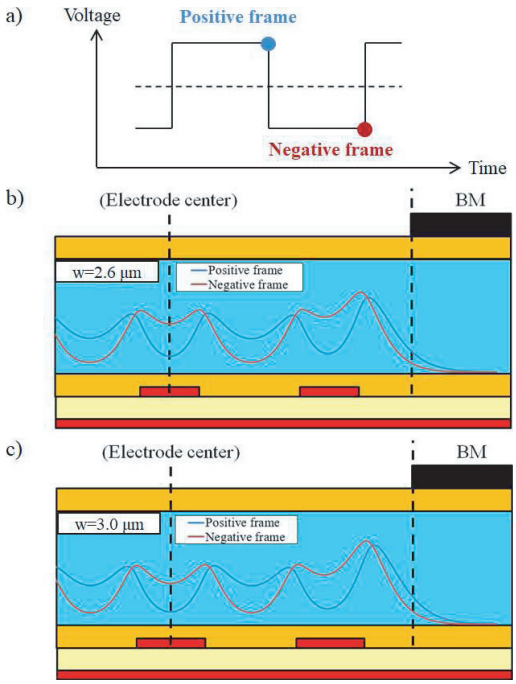

Fig. 19 Simulation results of pixel transmittance profile for positive and negative frames at 128 Gray level, a) Pixel applied voltage wave form image, b) pixel profile at w = 2.6 μm, and c) pixel profile at w = 3.0 μm

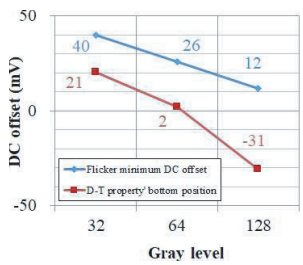

Fig. 20 Measurement results of flicker minimum DC voltage and D–T property bottom position

Fig. 19), both transmittance are not the same.

Thus we indicated that gray level dependences of D–T property bottom position and flicker minimum DC offset voltage due to the flexoelectric effect change depending on the slit electrode width or BM position. To optimize cell parameters, both of gray level dependences can be minimized.

Finally, we compare the measurement and simulation results at electrode width w = 2.4 μm, which is calculated using the data of w = 2.6 μm and w = 3.0 μm by extrapolation method. These results correspond well to each other at the point of inclination. The measurement results are shown in Fig. 20, which is the same as Fig. 9, and the simulation results are shown in Fig. 21.

Although the tendency of the gray levels of the two graphs is very similar, we confirm the difference, e.g. flicker minimum DC offset at 128 Gray is +10 mV in the measurement results, but that is about 0 mV in the simulation results. Considering the difference, we believe that there is some charging in some layer or on some interface between

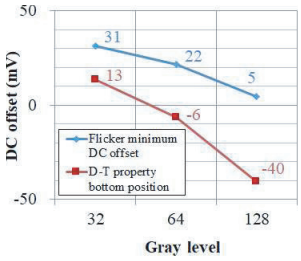

Fig. 21 Simulation results of flicker minimum DC voltage and D–T property bottom position; w = 2.4 μm, BM left edge position = 11 μm

the pixel and common electrodes. There is a possibility that this charging affects flicker shift in FFS mode.

4. Conclusion

In this paper, we discussed the image sticking and flicker (or flicker shift) phenomenon in the FFS mode LCD from several viewpoints.

The image sticking caused by residual DC (RDC) voltage is discussed in the viewpoints of DC offset–transmittance (D–T) property, which varied like a quadratic function and the JND (just noticeable difference) of brightness, which changed depending on the brightness of gray level. Although the width of the D–T properties at low gray levels are bigger than that at 128 Gray level, we demonstrated that the D–T property is defined by not only the changing ratio of V–T property but also the LC response property. Taking the influence of the JND into consideration, we found that image sticking caused by RDC is more visible at low gray levels than at 128 Gray level.

We also indicated that the D–T property bottom position varies depending on the gray level due to the flexoelectric effect. Although the flicker minimum DC offset voltage varies depending on the gray level due to the flexoelectric effect, both of the gray level dependences can be minimized by optimizing the electrode width and BM position. We verified that flicker factors can separate the flexoelectric effect and other effects to compare the measurement and simulation results of the D–T property and flicker minimum DC offset voltage at the same time.

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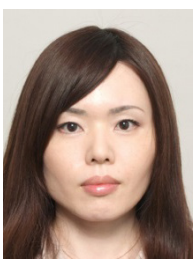

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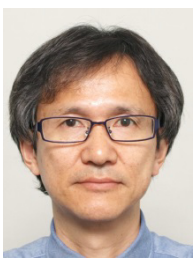

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