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High-Power High-Efficiency GaN HEMT Doherty Amplifiers for Base Station Applications

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SUMMARY In this paper, the high-power high-efficiency asymmetric Doherty power amplifiers based on high-voltage GaN HEMT devices with internal input matching for base station applications are proposed and described. For a three-way 1:2 asymmetric Doherty structures, an exceptionally high output power of 1 kW with a peak efficiency of 83% and a linear flat power gain of about 15 dB was achieved in a frequency band of 2.11–2.17 GHz, whereas an output power of 59.5 dBm with a peak efficiency of 78% and linear power gain of 12 dB and an output power of 59.2 dBm with a peak efficiency of 65% and a linear power gain of 13 dB were obtained across 1.8–2.2 GHz. To provide a high-efficiency broadband operation, the concept of inverted Doherty structure is applied and described in detail. By using a high-power broadband inverted Doherty amplifier architecture with a 2 × 120-W GaN HEMT transistor, a saturated power of greater than 54 dBm, a linear power gain of greater than 13 dB and a drain efficiency of greater than 50% at 7-dB power backoff in a frequency bandwidth of 1.8–2.7 GHz were obtained.

key words: *Doherty amplifier, asymmetric, inverted, broadband, GaN HEMT, efficiency*

1. Introduction

In next generation 5G telecommunication systems, it is required that the power amplifier operate with high power and high efficiency in a particular frequency band or over a wide frequency range to provide multiband and multistandard operation. Besides, in these systems with increased bandwidth and high data rate using OFDM transmission mode, the transmitting signal is characterized by high peak-to-average power ratio (*PAR*) due to wide and rapid variations of the instantaneous transmitting power. Therefore, it is especially important to provide high efficiency at maximum output power and at lower power levels typically ranging from −6 dB backoff or less over a wide frequency bandwidth. By using GaN HEMT technology and innovative Doherty architectures, drain efficiencies of 50–60% for average output powers up to 120 W can be achieved, thus reducing cost, size, and power consumption of the cellular transmitters.

The advantageous characteristics of the GaN HEMT include high breakdown voltage, high current density, high transition frequency (f_T), low on-state resistance, and low parasitic capacitance which result in a high-power, wide-bandwidth and high operation efficiency. The high-power density enables physically compact designs, while high dc-supply voltage operation and low parasitic output capacitance result in higher load impedance providing ease in obtaining wide bandwidths of operation. The drain-to-source breakdown voltage more than 150 V enables rugged operation at 50 V regardless of drive level or harmonic load environment. The Sumitomo GaN HEMT technology can provide high-gain operation of a packaged device at output power levels up to 300 W at operating frequencies over 8 GHz and beyond for radar applications and can result in excellent reliable performance for cellular high-power transmitters. The progress in power density of current generation devices of 5 W/mm made possible to reach 10 W/mm at 50-V operation. The use of SiC substrate results in an exceptionally good thermal performance.

For a conventional Doherty amplifier with a quarterwave impedance transformer and a quarterwave output combiner, the measured efficiency of 31% at backoff power levels of 6–7 dB from the saturated output power of about 43 dBm was achieved across the frequency range of 1.5–2.14 GHz [1]. To improve the broadband performance of a conventional Doherty amplifier, an output network can be composed of two quarterwave impedance inverters with reduced impedance transformation ratios [2]. For broadband combining, an output quarterwave transmission line with fixed characteristic impedance can be replaced with a multisection transmission line with different characteristic impedances and electrical lengths of its sections, which allow covering the frequency range from 2.2 to 2.96 GHz [3]. A high peak power of 500 W was achieved across the lower frequency band of 760–960 MHz using modified combining scheme with two quarterwave microstrip lines in the peaking amplifying path [4]. Using an asymmetric Doherty architecture, a saturated power of more than 270 W and a linear gain of more than 13 dB with a drain efficiency of more than 45% at 8-dB backoff points were achieved across the frequency range of 2.5–2.7 GHz [5]. A peak output power of 153–205 W and a drain efficiency varying within 40–60% at 6-dB backoff power level were achieved across the wide frequency band of 1.6–2.25 GHz, with an average power of 28 W and a drain efficiency of 50% for a single-carrier LTE signal with a *PAR* of 7.3 dB [6].

This paper introduces and describes high-power and high-efficiency broadband Doherty amplifier structures based on high-power GaN HEMT devices operating in a frequency bandwidth of 1.8–2.7 GHz for base station applications, which allows high efficiency across a wide fre-

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quency range and backoff output powers to be achieved using sufficiently compact and simple transmission-line load networks.

2. Symmetric and Asymmetric Doherty Amplifiers

There is a possibility to extend the region of high efficiency over a wider range of output powers if the carrier and peaking amplifiers are designed to operate with different output powers: smaller for the carrier amplifier and larger for the peaking amplifier. For instance, for a power division ratio of 1:2, the transition point with maximum drain efficiency corresponds to the backoff power level of about −9.5 dB from peak output power [7]. In this case, if for the symmetric Doherty structure shown in Fig. 1 (*a*) with 50-Ω load impedances seen by the carrier (CA) and peaking (PA) amplifiers, respectively, the characteristic impedance Z_T of the output quarterwave impedance transformer will be equal to $Z_T = 50/\sqrt{2} = 35.4\ \Omega$, then $Z_T = 50/\sqrt{3} = 28.9\ \Omega$ for an 1:2 asymmetric Doherty structure, as shown in Fig. 1 (*b*).

From Fig. 2, it follows that, for an asymmetric (1:2) Doherty amplifier, the maximum efficiency can be achieved at the saturation and 9.5-dB power backoff with sufficiently high efficiencies between these power levels. At the same time, such an asymmetric Doherty structure is substantially easier in implementation having much smaller size, compared to multistage Doherty configurations [8], [9], especially when considering different three-stage and four-stage symmetrical Doherty amplifier architectures [10]–[13]. The conventional Class-AB power amplifiers designed for the same application normally have the drain efficiencies about four times lower at this backoff power.

To optimize linearity and efficiency of the asymmetric Doherty amplifier, it is especially important to optimize the biasing conditions for the carrier and peaking amplifiers [14]. For two-way and three-way Doherty amplifiers with optimized individual bias conditions and load matching for the carrier and peaking amplifiers, applying an uneven drive results in more linear operation and produces more power than an even drive [15], [16].

For the packaged devices when it is difficult to choose a proper power ratio between the devices, it is convenient to use the identical power amplifiers that can compose ideally the N-way Doherty architecture where one carrier amplifier is in parallel with $(N-1)$ numbers of the peaking amplifiers. This is the simplest hybrid approach to acquire an $(N-1)$ times larger-sized peaking amplifier compared with the carrier amplifier for an asymmetric two-way ($N = 3$) Doherty amplifier configuration [17]. Figure 3 (*a*) shows the schematic diagram of an N-way Doherty amplifier with a parallel connection of one carrier amplifier and $(N-1)$ identical peaking amplifiers. The ideal drain efficiencies of the N-way Doherty amplifier (DA) architectures with peak values at −6 dB, −9.5 dB, and −12 dB power backoff points according to $P_{backoff} = 20\log_{10} N$ for the two-, three-, and four-way structures, respectively, are shown in Fig. 3 (*b*).

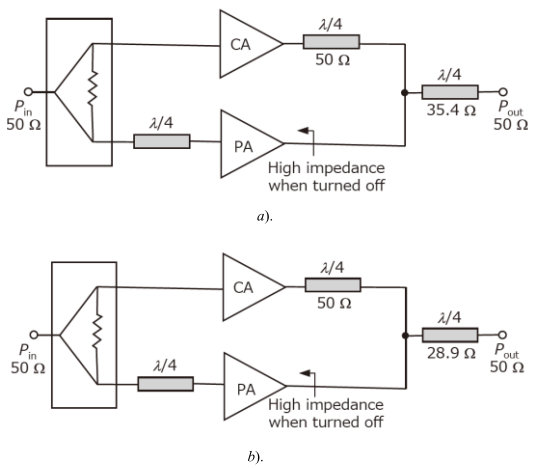

Fig. 1 Block schematics of (*a*) symmetric and (*b*) asymmetric 1:2 Doherty amplifier.

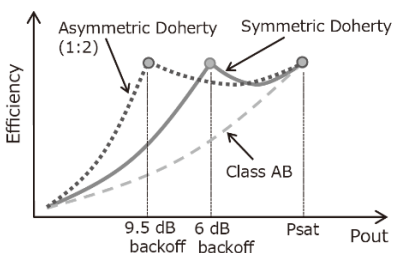

Fig. 2 Efficiency performance of symmetric and asymmetric 1:2 Doherty amplifier.

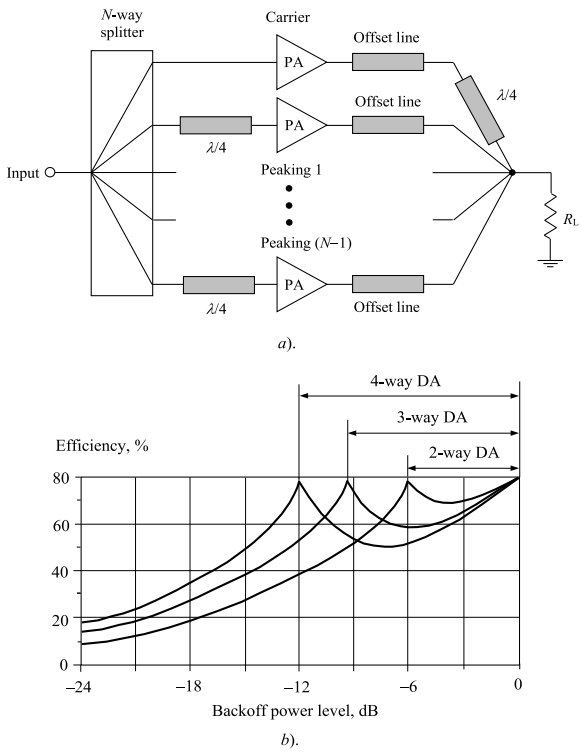

Fig. 3 Asymmetric multi-way Doherty amplifier and efficiencies.

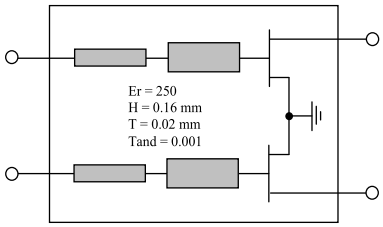

Fig. 4 Dual-path package with broadband input matching.

3. Packaged Device with Input Matching

A high-power operation of the GaN HEMT device can be achieved with larger gate periphery resulting in a greater power capability in given package. The corresponding increase in the gate-source capacitance when multiplicity of basic device cells is connected in parallel reduces the optimum input impedance to extremely low values, close to one or a few tenths of ohm. Therefore, a low-loss matching network is required inside the package to transform the impedance from the package lead reference plane to the device die reference plane. For practical use, it is required that the packaged power device should provide reasonable high ($> 1\ \Omega$) input impedance with a sufficiently low Q-factor to provide flat or initially specified performance over the required frequency bandwidth.

Depending on the package space availability and providing sufficiently wide operation bandwidth up to 40%, a two-stepped microstrip line on a high-permittivity ceramic substrate might be considered, as shown in Fig. 4 for a dual-path package where two separate GaN HEMT dies are attached in parallel. Such a two-stepped microstrip-line transformer for each device can transform the device input impedance of a few tenth of ohm to the input impedance of several ohms with flat or prescribed response and high return loss for 120-W device across the entire frequency bandwidth of 1.8–2.7 GHz or for 180-W device over 1.8–2.2 GHz. The partially pre-matched input impedance then should be transformed to 50-Ω termination with a sufficient accuracy over operating frequency bandwidth provided the unconventional stability conditions are satisfied with a load termination including Doherty power combiner.

The load pulling of an amplifying path (including packaging parameters) where two 50-V 180W dies are connected in parallel and biased in a Class-AB mode resulted in the contours of Fig. 5, which demonstrates the tradeoff in determining an optimum output match because the optimum impedance for maximum power (gray curves) is quite different than that for maximum efficiency (black curves). In this case, the output power at 1-dB gain compression achieves a maximum of about 55 dBm at a low impedance condition of $(1.2 - j1.1)\ \Omega$, whereas a maximum efficiency of 61.7% is obtained for a purely resistive impedance of about 1.3 Ω, as shown in Fig. 5.

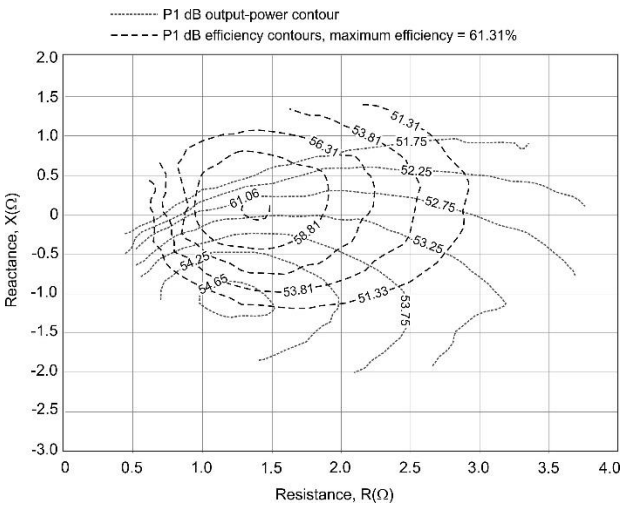

Fig. 5 Load-pull output power and efficiency contours.

4. 1-kW High-Efficiency 2.11–2.17 GHz Doherty Amplifier

As devices with high output power have lower impedance in general, the width of microstrip lines of external matching circuits becomes large. Besides, to realize wideband characteristics, an impedance conversion ratio needs to be small, resulting in an external circuit designed in a low impedance system. In Doherty amplifiers, if wide microstrip lines are used, it can be quite difficult to physically connect the outputs of the peaking amplifier and carrier amplifier [18]. Adding a half-wavelength line at the peaking amplifier output can increase the flexibility of the circuit layout without losing the Doherty operation. To align the phases of both the carrier and peaking amplifiers, an additional $\lambda/4$ length line needs to be incorporated at the input side of the carrier amplifier. An example of this configuration with an asymmetric power ratio of 1:2 is shown in Fig. 6 (*a*).

For the packaged high-power devices when it is difficult to choose the proper power ratio between the devices, it is convenient to use the identical power amplifiers which can compose ideally the multi-way Doherty architecture where one carrier power amplifier is in parallel with multiple peaking amplifiers. As a result, a 1:2 asymmetric two-way Doherty structure can be transformed to a modified three-way asymmetric Doherty configuration with one carrier amplifying path and two identical peaking amplifying paths when device sizes for the carrier amplifier (CA) and both peaking amplifiers (PA1 and PA2) are equal, as shown in Fig. 6 (*b*). Here, the half-wave line in each peaking amplifying path can be split into two quarterwave lines, each having its own characteristic impedance for the corresponding impedance transformation when the required load impedance for peaking device is sufficiently small.

Figure 7 shows the final block schematic of a three-way asymmetric Doherty amplifier configuration, where the output combiner includes one $\lambda/4$ microstrip line in a car-

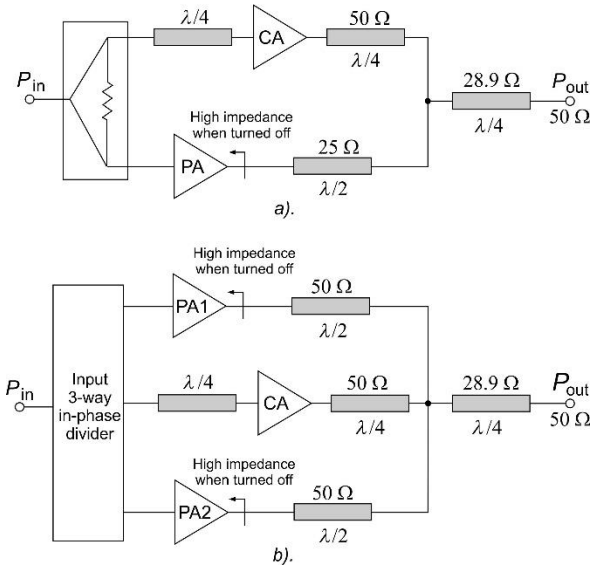

Fig. 6 Block schematics of modified 1:2 asymmetric Doherty amplifier.

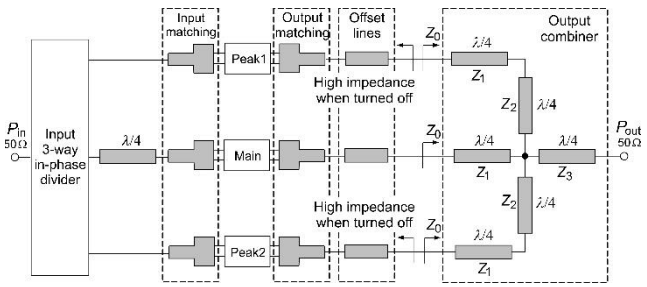

Fig. 7 Block schematic of high-power 2.11–2.17 GHz Doherty amplifier.

rier path, two $\lambda/4$ microstrip lines in each peaking path, and one combining $\lambda/4$ microstrip line [19]. Here, each amplifying path includes the packaged device of the same die size, input and output matching circuits using microstrip lines. Offset lines are necessary to provide open-circuit conditions at their ends for peaking amplifiers when they are turned off. Then, two quarterwave microstrip lines with different widths required for the corresponding impedance transformation translate this open-circuit condition in each peaking path to open circuit seen by the carrier path at output power levels higher than −9 dBc at a common node in the output combiner. For example, for identical amplifiers having optimum load impedance $Z_0 = 12\ \Omega$ each and $Z_2 = R_L = 50\ \Omega$, where R_L is the standard 50-Ω load impedance, $Z_1 = \sqrt{Z_0 Z_2} = 24.5\ \Omega$ and $Z_3 = \sqrt{Z_2 R_L}/\sqrt{3} = 28.9\ \Omega$. There may be different combinations of the characteristic impedances between quarterwave microstrip lines in the output combiner. The quarterwave microstrip line in the input path of the carrier amplifier is used to compensate for the delay provided by the output combiner.

The test board of a modified three-way Doherty amplifier based on three dual-path GaN HEMT devices in metal-ceramic flange packages, each including a pair of 180-W Sumitomo GaN HEMT dies with internal input matching,

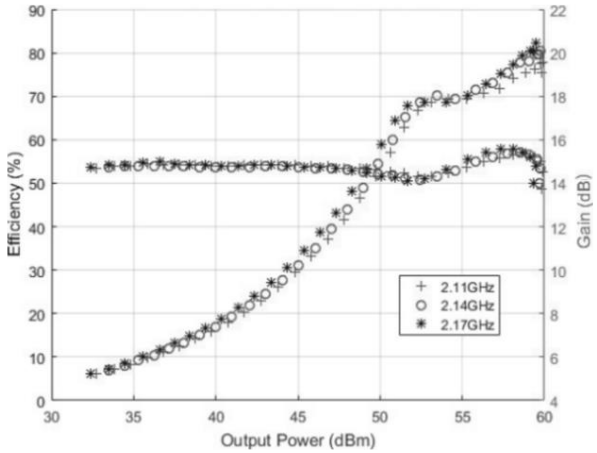

Fig. 8 Measured results of 2.11–2.17 GHz Doherty amplifier.

was fabricated on a 20-mil RO4350 substrate. The input three-way divider, input and output matching circuits, offset lines, output combiner, and gate and drain bias circuits (having bypass capacitors on their ends) are fully based on microstrip lines of different electrical lengths and characteristic impedances.

As a result, the measured saturated output power P_{sat} = 59.5 dBm and peak efficiency of 78% with a power gain of about 14 dB were achieved at a supply voltage of 55 V within the frequency range of 2.11–2.17 GHz. Figure 8 shows the plots of the drain efficiency versus output power, with a drain efficiency of about 60% at around −9 dB power backoff level. For a 20-MHz LTE signal with 9-dB *PAR*, an average output power of 50 dBm was obtained with a drain efficiency of 55.0% [20]. In this case, a power gain of about 15 dB was achieved in a linear operating region having 2-dB flatness over the entire output power range up to 59.5 dBm when its value reduces by just 1 dB, compared to its value in linear region, as shown in Fig. 8.

5. High-Power 1.8–2.2 GHz Doherty Amplifier

However, wider frequency bandwidth can also be achieved by using an asymmetric two-way or three-way Doherty structure [21], [22]. On the basis of an accurate load-pull testing and practical implementation of an asymmetric two-way Doherty amplifier, an average power of 85 W with a peak power of 470–570 W and relatively flat average efficiency of 45–49% was achieved across the frequency band of 1.8–2.2 GHz for a single-carrier 20-MHz WCDMA signal with a *PAR* of 10 dB [21].

The circuit implementation of a high-power asymmetric three-way 1.8–2.2 GHz GaN HEMT Doherty amplifier where a half-wave microstrip line is included into the load network of each identical peaking path for better flexibility in practical implementation is shown in Fig. 9, while providing sufficient bandwidth capability at the same time [20], [23].

In Fig. 9, the microstrip line ($\lambda/4 + \lambda/2$) with a total electrical length of 270° at the carrier (main) amplifier out-

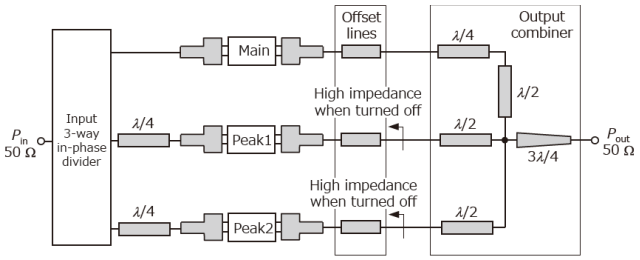

Fig. 9 Block schematic of high-power 1.8–2.2 GHz Doherty amplifier.

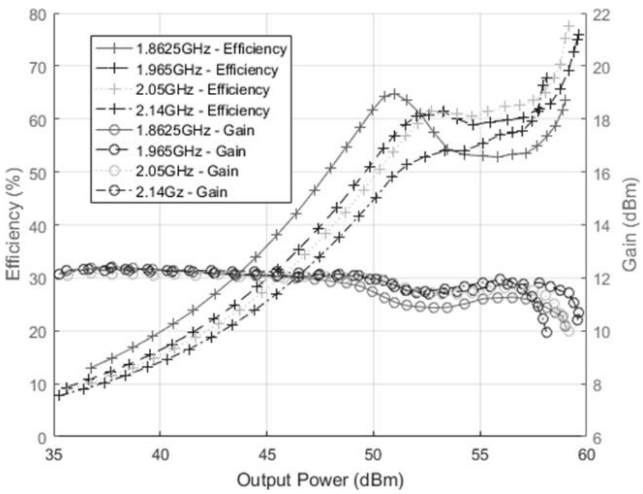

Fig. 10 Efficiency and power gain of high-power 1.8–2.2 GHz Doherty amplifier.

put to provide the corresponding impedance transformation at significant power backoff and the quarterwave microstrip line in each input path of the peaking amplifiers to compensate for the delay provided by the output combiner are used. The broadband output impedance transformation with a 50-Ω load is provided by using a Klopfenstein taper having an electrical length of 270° at center bandwidth frequency.

The test board of a three-way Doherty amplifier based on three dual-path 180-W Sumitomo GaN HEMT devices in metal-ceramic flange packages, was fabricated on a 20-mil RO4350 substrate. The peak output power P_{2dB} of 59.5 dBm at 2-dB gain compression point and peak efficiency of 78% with a linear flat power gain of about 12 dB were measured at a supply voltage of 55 V within the frequency range of 1.8–2.2 GHz, as shown in Fig. 10. From the test results, it follows that the drain efficiency of greater than 50% at 8-dB power backoff can be achieved. This means that, for a 20-MHz LTE signal with 8-dB *PAR*, an average power of 120 W can be obtained with a drain efficiency of equal or greater than 50% over the most part of the entire frequency range.

6. Inverted Doherty Amplifier Configuration

An inverted Doherty amplifier structure is an alternative configuration when, in view of presence of the parasitic device drain-source capacitance and series bondwire and package lead inductance, it can be easier to provide a short circuit rather than an open circuit at the output of the peaking amplifier when it is turned off. The block schematic diagram of an inverted Doherty amplifier configuration with an impedance inverter based on a quarterwave transmission line connected to the output of the peaking amplifier is shown in Fig. 11. The quarterwave transmission line can also be implemented in a compact form suitable for use in mobile applications [24]. In this case, a quarterwave transmission line operating as an impedance inverter is used at low-power levels to transform sufficiently low device output impedance after the offset line to high impedance seen from the junction point where both peaking and carrier amplifying paths are directly connected followed by an optimized output quarterwave transmission-line transformer or matching circuit [25], [26]. Because the quarterwave transmission line is now physically presented in a peaking amplifying path rather than in a carrier amplifying path corresponding to a conventional structure, such a Doherty amplifier was called an inverted Doherty amplifier, although impedance matching in a carrier amplifying path to increase impedance seen by the carrier device at low-power region is provided by the corresponding output matching circuit, or in a simplified case, by a lumped low-pass L-type transformer consisting of the shunt drain-source capacitance and series bondwire and package lead inductance.

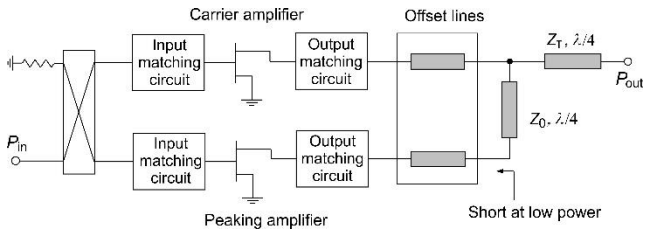

Fig. 11 Block schematic of inverted Doherty amplifier.

To better understand the operation principle of an inverted Doherty amplifier, consider separately the load network shown in Fig. 12 (*a*), where the peaking amplifier is turned off. In a low-power region, the phase adjustment of the offset line with electrical length θ causes the peaking amplifier to be short-circuited (ideally equal to 0 Ω), and the matching circuit in conjunction with offset line provides the required impedance transformation from 25 Ω to the optimum high impedance Z_{opt} seen by the carrier device output at the 6-dB power backoff, as shown in Fig. 12 (*b*). In this case, the short circuit at the end of the quarterwave line transforms to the open circuit at its input so that it prevents power leakage to the peaking path when the peaking transistor is turned off. In a high-power region, both the carrier and peaking amplifiers are operated in a 50-Ω environment in parallel, and the output quarterwave line with the characteristic impedance of 35.4 Ω transforms the obtained 25 Ω to the required 50-Ω load.

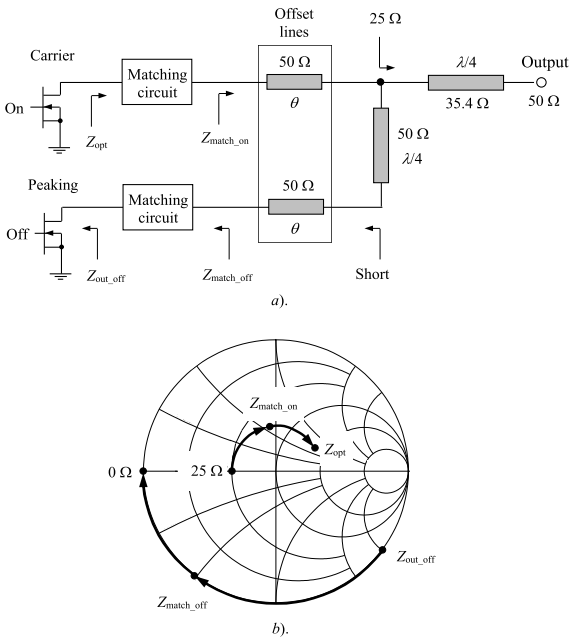

Fig. 12 Load network of inverted Doherty amplifier and Smith chart impedances.

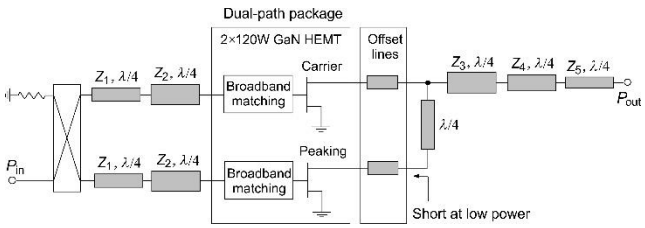

Fig. 13 Block schematic of broadband inverted Doherty amplifier.

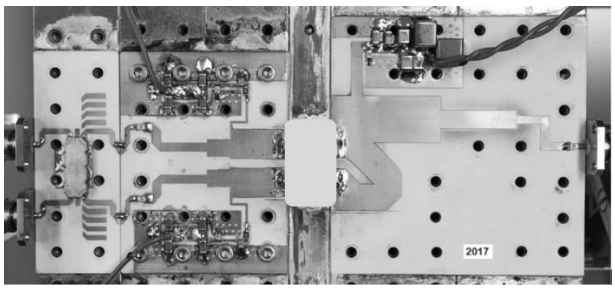

Fig. 14 Test board of broadband 1.8–2.7 GHz inverted Doherty amplifier.

7. Broadband 1.8–2.7 GHz Inverted Doherty Amplifier

By using an inverted Doherty architecture, broadband performance can be achieved when a multisection broadband impedance transformer can be used instead of a quarterwave output impedance transformer. The first broadband 1.8–2.7 GHz transmission-line GaN HEMT inverted Doherty amplifier was fabricated on a 20-mil RO4360 substrate using two Cree GaN HEMT CGH40010P devices and commercially available broadband coupled-line coupler. For a single-carrier 5-MHz WCDMA signal with a *PAR* of 6.5 dB, the drain efficiencies of 58%, 50%, and 42% at an average output power of 38 dBm with a power gain over 11 dB were achieved at the operating frequencies of 1.85 GHz, 2.15 GHz, and 2.65 GHz, respectively, with an *ACLR* (at 5-MHz offset) measured from −32 dBc at 1.85 GHz to −37 dBc at 2.65 GHz [27].

However, much higher output power level over a very wide frequency range can also be achieved using such a broadband inverted architecture of the Doherty amplifier [28]. By using two 80-W Sumitomo GaN HEMT devices, the drain efficiency of 51% with an average total output power of 45.5 dBm (18.2 W for 1.85-GHz GSM signal and 17 W for 10-MHz 2.65-GHz LTE signal) with an *ACLR* of −57 dBc and the drain efficiency of 43% at an average total output power of 44.8 dBm (two equal 20-MHz LTE signals with a *PAR* of 7.2 dB spaced by 460 MHz) with an *ACLR* of −53 dBc were measured using DPD linearization.

Figure 13 shows the schematic diagram of an inverted broadband Doherty amplifier configuration based on a dual-package transistor having two 120-W Sumitomo GaN HEMT devices with internal input matching and a quarterwave line connected to the output of the peaking amplifier. Such an inverted architecture can be very helpful if, in a low-power region, it is easier to provide a short circuit rather than an open circuit at the output of the peaking amplifier which depends on the characteristics of the transistor. External input broadband matching technique using two quarterwave lines with different characteristic impedances is used in each carrier and peaking path.

In this case, a quarterwave line is used to transform extremely low output impedance after the offset line to high impedance seen from the carrier path at the load junction. To cover the frequency range of 1.8–2.7 GHz, the output broadband impedance-transforming network consists of three $\lambda/4$ lines with different values of their characteristic impedances, in order of decreasing from the 50-Ω load to the common node for carrier and peaking paths.

Figure 14 shows the test board of an inverted broadband Doherty amplifier configuration based on two 120-W Sumitomo GaN HEMT devices in a single dual-path package with internal input matching and a wide quarterwave microstrip line connected to the output of the peaking amplifier [29]. Here, the commercially available broadband 3-dB coupler is used to equally split input power, input broadband matching technique using multisection microstrip lines with different characteristic impedances in both the carrier and peaking amplifying paths and the output broadband impedance-transforming network consisting of three quarterwave microstrip lines with different values of their characteristic impedances line were used to cover the frequency range of 1.8–2.7 GHz.

Figure 15 shows the measured power gain and drain efficiency of such a broadband high-power transmission-line GaN HEMT inverted Doherty amplifier fabricated on a 20-mil RO4350 substrate across the frequency bandwidth of

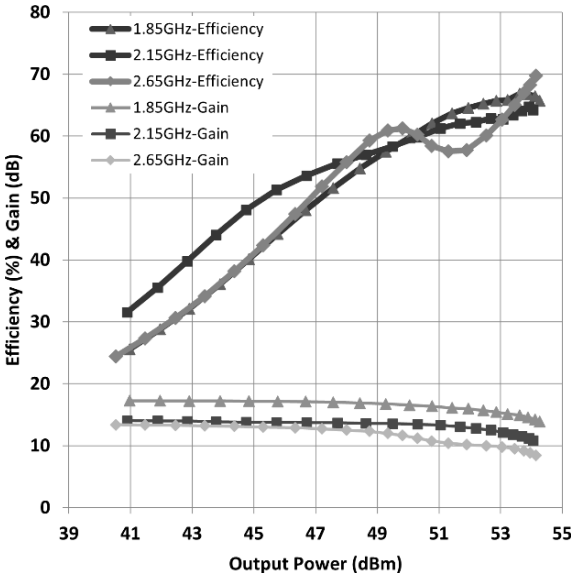

Fig. 15 Efficiency and power gain of broadband 1.8–2.7 GHz inverted Doherty amplifier.

1.8–2.7 GHz. In this case, a linear power gain over 13 dB was achieved in an entire frequency range. At the same time, the drain efficiencies over 65% at saturation power $P_{3dB} > 54$ dBm and over 50% at 7-dB backoff output powers were measured across the entire frequency bandwidth at a dc-supply voltage of 55 V, with a maximum drain efficiency of about 70% at higher bandwidth frequency.

For comparison, by using similar approach for designing a broadband inverted Doherty amplifier based on two Cree GaN HEMT CGHV40100 devices with additional harmonic tuning, a drain efficiency of 40.0–50.2% at 6-dB backoff with a saturation output power of 52.7–54.3 dBm and a power gain varying from about 14 dB in a linear region to lower than 7 dB at saturation was obtained across the frequency bandwidth of 1.7–2.7 GHz, with a drain efficiency around 45% at an average output power of 46 dBm for a single-carrier 10-MHz LTE signal with a *PAR* of 7.5 dB [30].

An additional difficulty to design the broadband transistor power amplifier apart from the broadband impedance transformation with large impedance ratio and prescribed reactive constraints is that the matching networks must be designed with prescribed tapered magnitude characteristics to compensate for the transistor gain roll-off at higher frequencies that is inherent with any type of transistors. The gain tapering is a direct consequence of the fact that the transistor maximum available gain decreases with increasing frequency. Thus, for a flat overall gain response, matching networks with tapered magnitude characteristics must be used, where the exact frequency dependence of the taper or gain slope varies with specific types of transistors.

8. Conclusion

The high-power high-efficiency broadband Doherty power amplifiers based on high-power GaN HEMT devices with internal input matching for base station applications are proposed and described. For a three-way Doherty implementation using three 2 × 180-W Sumitomo GaN HEMT transistors, an exceptionally high output power of 59.5 dBm corresponding to 2-dB gain compression point with a peak efficiency of 78%, drain efficiency of greater than 50% at 8-dB power backoff and a linear flat power gain of about 12 dB were achieved across 1.8–2.2 GHz. By using a high-power broadband inverted Doherty amplifier architecture with a 2 × 120-W Sumitomo GaN HEMT transistor, a saturated power of greater than 54 dBm, a linear power gain of greater than 13 dB and a drain efficiency of greater than 50% at 7-dB power backoff in a frequency bandwidth of 1.8–2.7 GHz were obtained.

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