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A Study on Highly Efficient Dual-Input Power Amplifiers for Large PAPR Signals

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SUMMARY With the advent of 5G and external pressure to reduce greenhouse gas emissions, wireless transceivers with low power consumption are strongly desired for future cellular systems. At the same time, increased modulation order due to the evolution of cellular systems will force power amplifiers to operate at much larger output power back-off to prevent EVM degradation. This paper begins with an analysis of load modulation and asymmetrical Doherty amplifiers. Measurement results will show an apparent 60% efficiency plateau for modulated signals with a large peak-to-average power ratio (PAPR). To exceed this efficiency limitation, the second part of this paper focuses on a new amplification topology based on the amalgamation between Doherty and outphasing. Measurement results of the proposed Doherty-outphasing power amplifier (DOPA) will confirm the feasibility of the approach with a modulated efficiency greater than 70% measured at 10 dB output power back-off.

key words: *Doherty amplifier, outphasing amplifier, Doherty-outphasing amplifier, base stations, multiple-input amplifier*

1. Introduction

5G ultra-high capacity, massive machine type communication and ultra-low latency systems are beginning to be brought online and discussions on beyond-5G or 6G are also starting to take place. With the rapid evolution of information and communication systems, the volume of information transmission is expected to increase rapidly. As a result, it has been estimated based on data from 2016 that the power consumption of IT equipment including wireless transceivers will increase 36 times by 2030 [1], [2]. Focusing on the base stations for cellular systems, the authors from [3] reported that the power amplifier accounts for 60% of the total power consumption. In addition, based on the Paris Agreement, the world is beginning to move towards decarbonization [4]. Considering the trend of rapid increases in power consumption to meet demand and the external pressure to improve power efficiency, power amplifiers with low power consumption should be strongly promoted.

Orthogonal frequency division multiplexing (OFDM) signals used in cellular systems typically have a large PAPR, which is theoretically equivalent to that of a complex Gaussian signal. Therefore, power amplifiers used to amplify such signals operate on average at output power levels much smaller than saturation. In such systems, the instantaneous efficiency near the average output power level becomes dominant, which is typically worse than at saturation. At the same time, increases in modulation order due to the continuous evolution of cellular systems will force power amplifiers to operate at even larger output power back-off to prevent EVM degradation. As a result, further impacting the efficiency performance of power amplifiers.

Driven by further enhancing the efficiency performance, power amplifiers have evolved from class-A to class-B and ultimately into the classical two-way Doherty amplifier topology [5]–[9] where focus has been placed on the efficiency away from output power saturation. In addition, three-way Doherty amplifiers [10]–[13] have also been reported as an extension of two-way Doherty amplifiers. Doherty amplifiers are typically single-input and three-way Doherty amplifiers are the most cost-effective at the moment. According to the results of previous papers, the average efficiency at 10 dB output power back-off has plateaued at around 60% [7], [10]. The 60% efficiency plateau is not necessarily caused by a circuit limit, but because the activities on PA research in recent years have mainly focused on bandwidth expansion rather than efficiency improvement.

Although single-input power amplifiers are inherently plug-and-play like and hence easily upgradable, to enable alternative methods of efficiency enhancement, multiple-input power amplifiers have become more popular in recent years. Multiple-input power amplifiers include envelope tracking (ET) [14]/envelope elimination and restoration (EER) [15] power amplifiers (PAs), dynamic load modulation (DLM) PAs [16]–[18], dual-input Doherty amplifiers [19] and outphasing amplifiers [20]–[24]. ET/EER PAs, which improve the efficiency by modulating the supply voltage, require an envelope modulator, which is a complex circuit to modulate the power supply. DLM-PAs require tunable matching networks typically implemented using varactor diodes, which utilize a control voltage of 10 V or more. The control voltage is usually coupled from the input signal. Outphasing amplifiers are implemented using two RF amplifiers and a Chireix combiner for combining the output signals of the amplifiers.

What all multiple-input power amplifier have in common is that extra digital signal processing is required to generate additional input signals from the original source

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signal. As can be seen in previous reports of multiple-input PAs [10], [14], none of them have achieved efficiencies much higher than the Doherty amplifier at an output back-off level larger than 9 dB. It should be noted that the improvement benefit of the multiple-input scheme applied to Doherty amplifiers is limited because only a single amplifier from the two or more total amplifiers operates at large output power back-off levels.

Since outphasing amplifiers can be realized with the combination of RF circuits and digital signal processing, the system is simpler than either the ET/EER PA or the DLM PA. Furthermore, the Chireix combiner can be designed independently of the two amplifier blocks. As such, unique architecture implementations are possible. A dual-input architecture using two Doherty amplifiers as the branch amplifiers of an outphasing amplifier was proposed and discussed in [25]. In this architecture, Doherty operation is used at low input power levels while outphasing is utilized at high output power levels. This is in contrast to the work presented in [26] where outphasing operation is embedded into two parallel Doherty amplifiers. In this topology outphasing and Doherty operation are used at low and high input power levels respectively. This merged architecture of Doherty and outphasing yielded continuous wave (CW) efficiency of 50% at 12 dB output power back-off. Mixed-mode input signal drive optimization was applied to the topology presented in [26] with the performance results documented in [27].

Even with optimally embedding multiple efficiency optimization schemes into a single multiple-input amplifier architecture, modulated efficiency remains plateaued at around 60% [26], [27]. However, the Doherty-outphasing power amplifier (DOPA) proposed by the authors in [25] has shown that it is possible to attain 70% efficiency under 10 dB PAPR modulated signal conditions. However, it should be noted that this comes at the expense of a cost increase due to the additional circuit complexity of the multiple-input architecture. This paper will expand on the contents of [25] with additional theory and discussions regarding the design of the output combiner of the two Doherty amplifiers and how they can be effectively cascaded with the Chireix combiner to form a DOPA.

This paper is organized as follows. Section 2 will briefly introduce the theory behind load modulation and its application to amplifier design. This will then lead into Sect. 3 where the asymmetrical Doherty amplifier and two different implementations will be discussed. Section 4 will introduce the operating principle behind the DOPA along with both CW and modulated measurement results. Conclusions and final thoughts are given in Sect. 5.

2. Load Modulation Theory

A load modulated amplifier generally refers to an amplifier that dynamically changes the load impedance presented to the device in some way for the purpose of increasing power efficiency during back-off operation. The purpose of varying the load impedance is to make the device operate close to voltage saturation even under output power back-off operation for high efficiency. One way to achieve load modulation is by combining 2 or more amplifiers into a single common load as shown in Fig. 1. Here the field effect transistors (FETs) typically used for the design of amplifiers have been replaced by voltage controlled current sources for ease of analysis. The load impedance presented to each voltage controlled current source can be easily calculated by turning Fig. 1 into a two-port network.

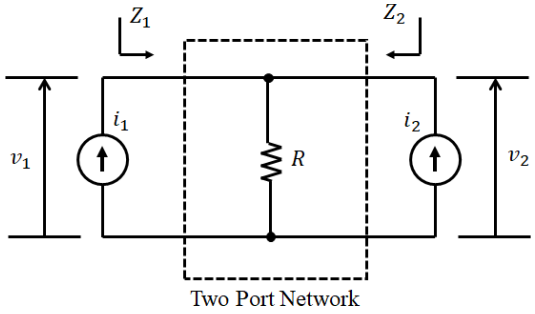

Fig. 1 Simplified analytical block diagram of a load modulated power amplifier

The relationship between the currents and voltages in the two-port network shown in Fig. 1 is expressed by Eq. (1) using Z-matrix notation.

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} R & R \\ R & R \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \tag{1}$$

From Eq. (1), the load impedance presented to each device can be expressed as

$$Z_1 = R\left(1 + \frac{i_2}{i_1}\right) \tag{2}$$

$$Z_2 = R\left(1 + \frac{i_1}{i_2}\right) \tag{3}$$

The impedances Z_1 and Z_2 can be varied or modulated by appropriately controlling the currents i_1 and i_2. However, it is rather obvious that in this configuration the voltage applied across both current sources is identical and increases with increases in either current i_1 or i_2. In other words, a constant voltage or voltage saturation under back-off operation is not realized.

To create a realistic amplifier topology that utilizes voltage saturation for efficiency enhancement, some form of decoupling between current and voltage is required. One way to achieve this is by using a non-isolated output combiner typically used in Doherty and outphasing amplifiers. This is illustrated in Fig. 2 where a quarter-wavelength transmission line provides the necessary conditions for voltage saturation in a Doherty amplifier. The Doherty amplifier consists of a carrier and peaking amplifier where the carrier amplifier operates at all input power levels while the peaking amplifier operates from middle to high input power levels [28]. In load modulated amplifiers such as Doherty amplifiers and outphasing amplifiers, the design must be

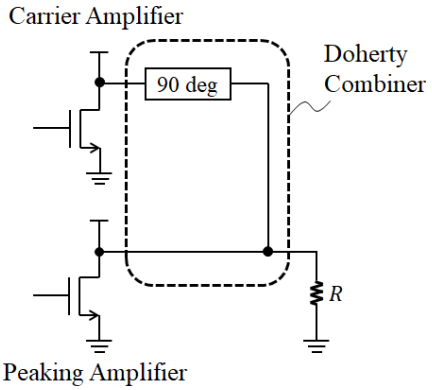

Fig. 2 Simplified block diagram of a Doherty amplifier

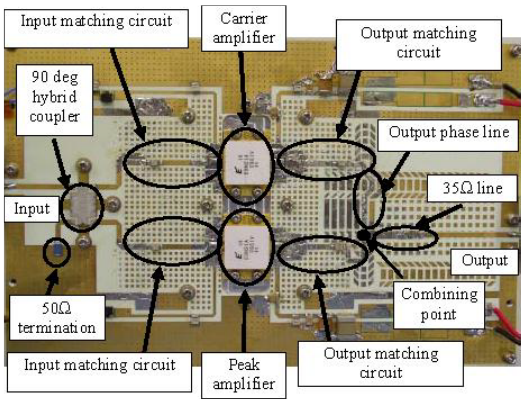

Fig. 3 Photograph of the fabricated Doherty amplifier with asymmetrical drain voltage [8]

based on the analytically calculated movement of the load impedances.

3. Asymmetrical Approach to Doherty Amplifiers

There is a limit to the potential efficiency enhancement possible with the aid of voltage saturation and load modulation. As shown in Eq. (2), the dynamic range of available load modulation presented to the first (carrier) amplifier is bound between R Ohms and $2R$ Ohms if the size of both the carrier and peaking amplifier are identical. In other words, currents i_1 and i_2 have the same maximum value. By increasing the maximum value of current i_2, the dynamic range of available load modulation can be expanded. This in turn provides a larger output power range where voltage saturation and hence efficiency enhancement occurs. In the case of a Doherty amplifier, this can be realized either by using a larger peaking device or by reducing the drain supply voltage of the carrier amplifier with respect to the peaking amplifier.

3.1 Doherty Amplifier with Asymmetrical Drain Voltage

An asymmetrical 2.15 GHz Doherty amplifier implemented using asymmetrical drain supply voltages is shown in Fig. 3 [8]. The same type of GaN HEMT with a saturation power of 210 W is used for both the carrier and peaking amplifier. The drain supply voltage of the carrier amplifier is 40 V, while that of the peaking amplifier is set asymmetrically at 50V.

Figure 4 shows the CW measurement results of the Doherty amplifier with an asymmetrical drain supply voltage compared to a Doherty amplifier with a symmetrical 50 V drain supply. The Doherty amplifier with an asymmetrical drain supply voltage has an improved efficiency performance of up to 10 percentage points when compared to the symmetrical supply voltage case. Furthermore, as discussed in [8], evaluation using WCDMA signals showed that the Doherty amplifier with an asymmetrical drain supply voltage improved the efficiency from 40% for a symmetrical drain supply voltage to 50% at 45 dBm output power, which is at 9 dB output power back-off level from saturation.

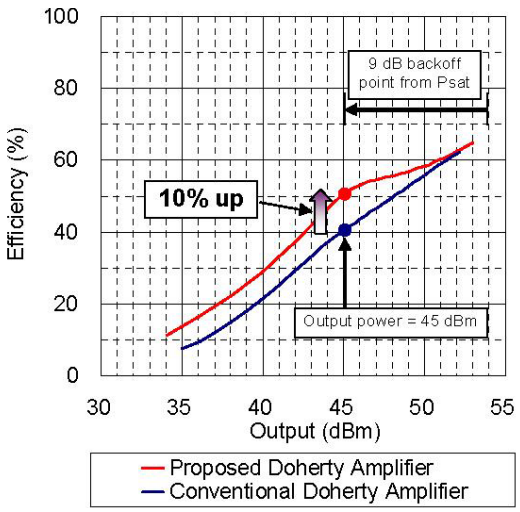

Fig. 4 CW measurement results of the asymmetrical drain supply voltage Doherty amplifier (dots) compared to the same Doherty amplifier with a symmetrical 50 V drain supply voltage (solid line) [8]

3.2 Doherty Amplifier with Asymmetrical Device Size

The second asymmetrical Doherty amplifier is implemented by doubling the size of the peaking amplifier with respect to the carrier amplifier for UHF band applications. This was realized by using three identical GaN HEMTs but combing two of them into a single peaking unit as shown in Fig. 5 [9]. The output signal of the two peaking amplifiers are combined by using a Wilkinson combiner. As a result, the total output power of the peaking unit is twice the output power of the carrier amplifier, resulting in an asymmetrical configuration equivalent to a 1:2 asymmetrical device size. The maximum output power ratio of the peaking amplifier to the carrier amplifier determines the output power of the first efficiency peak. The output power at which the first efficiency peak occurs relative to the saturated output power is expressed as

$$P_{BO} = 20\log_{10}(1+\gamma) \quad \text{(dB)} \tag{4}$$

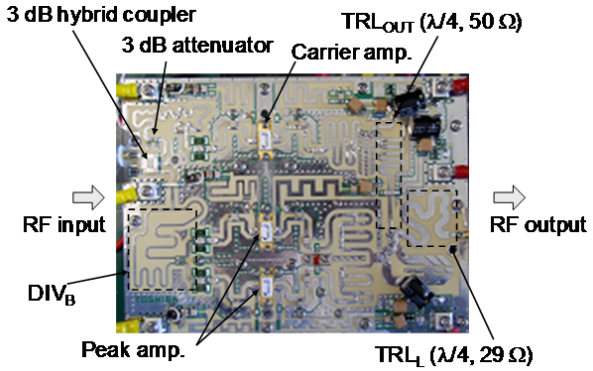

Fig. 5 Photograph of the fabricated Doherty amplifier with asymmetrical device size [9]

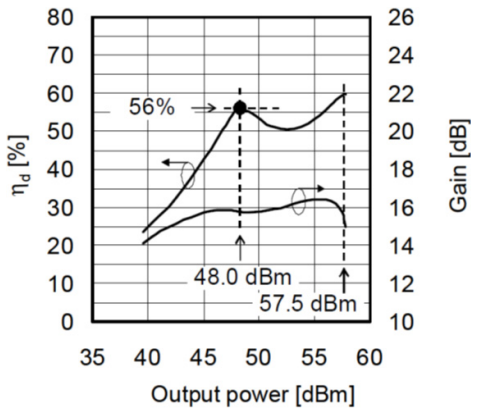

Fig. 6 CW measurement results by using CW signals for the 1:2 asymmetrical Doherty amplifier [9]

where γ is the maximum power ratio of the peaking amplifier with respect to the carrier amplifier. γ has a value of 2 for a 1:2 asymmetrical Doherty amplifier, resulting in P_{BO} of 9.5 dB.

Figure 6 shows the measured CW efficiency and gain. The saturation power was 57.5 dBm and the first efficiency peak of 56% occurred at 9.5 dB backed-off from saturation. Using a 9.5 dB PAPR 6 MHz OFDM signal, an average efficiency of 52% was measured with 48 dBm average output power.

4. Doherty-Outphasing Power Amplifier

Although various Doherty amplifiers have been developed, based on recent published work [7]–[10], it would be difficult to achieve a modulated efficiency better than 60% with a PAPR larger than 9 dB. Therefore, as a new approach, a DOPA, which is based on the mixed-signal outphasing amplifier and employs Doherty amplifiers as its branch amplifiers, has been developed [25], [29]. After a brief introduction to outphasing amplifiers and their mixed-mode operation, the proposed DOPA will be discussed in greater depth.

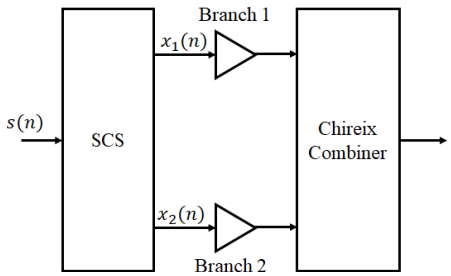

Fig. 7 Simplified block diagram of a typical outphasing amplifier that consists of an SCS, two branch amplifiers and a Chireix combiner

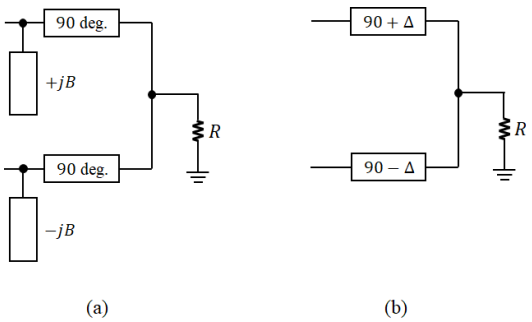

Fig. 8 Chireix combiner realization (a) shunt compensation (b) series compensation

4.1 Outphasing Amplifier

Figure 7 shows the simplified block diagram of an outphasing amplifier, where frequency converters are not described. The signal component separator (SCS) separates a complex baseband input signal at sample n, $s(n)$, into two complex baseband signals, $x_1(n)$ and $x_2(n)$, with constant amplitude $v_{\max}$, as follows.

$$x_1(n) = v_{\max} e^{j(p(n)+\phi(n))} \tag{5}$$

$$x_2(n) = v_{\max} e^{j(p(n)-\phi(n))} \tag{6}$$

$$\phi(n) = \arccos\left(\frac{|s(n)|}{2v_{\max}}\right) \tag{7}$$

$$p(n) = \arg(s(n)) \tag{8}$$

$\phi(n)$ is the phase difference between $x_1(n)$ and $s(n)$. The operation that converts $|s(n)|$ to $\phi(n)$ over the entire amplitude range is called pure-outphasing operation.

Like the Doherty combiner, the Chireix combiner is also a non-isolated combiner. This causes load modulation to occur at the output terminal of both branch amplifiers. However, unlike the Doherty amplifier, the load modulation caused by a Chireix combiner has a varying reactive component. As such reactive compensation is inherently embedded into the Chireix combiner. Two compensation circuit topologies exist, namely shunt and series compensation as shown in Fig. 8 (a) and Fig. 8 (b) respectively. B is the susceptance of the reactive elements in Fig. 8 (a) and Δ is the phase shift away from a quarter-wavelength in Fig. 8 (b).

The theoretical efficiencies of a Class B amplifier, a

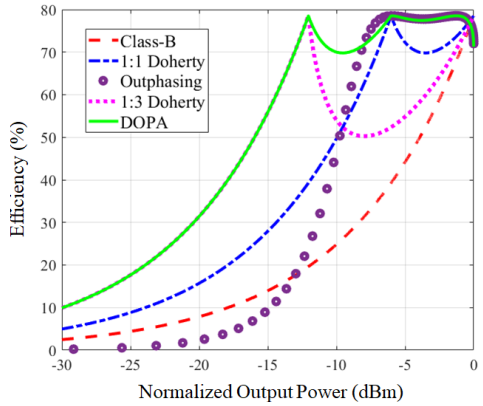

Fig. 9 Theoretical efficiencies of a class-B amplifier, a symmetrical Doherty amplifier, an outphasing amplifier, a 1:3 asymmetrical Doherty amplifier and the proposed DOPA with respect to normalized output power

symmetrical Doherty amplifier, and an Outphasing amplifier are shown in Fig. 9. For the symmetrical Doherty amplifier, the efficiency was calculated using a characteristic impedance of 50 Ohms for the 90-degree transmission line and 25 Ohms for the load. For the outphasing amplifier, the characteristic impedance of the 90-degree transmission line was set to 25 Ohms, the load to 50 Ohms, and the susceptance B to 0.07 Siemens.

This value of B ensured that the symmetrical Doherty and outphasing amplifier reach their first efficiency peak at the same output power back-off level. It is quickly apparent that unlike Doherty amplifiers, outphasing amplifiers have very little efficiency degradation between the two efficiency peaks. As such, 70% or more modulated efficiency can realistically be attained with signals whose PAPR is 7 dB or smaller [21], [23]. However, the efficiency at large output power back-off drops of steeply and is 10 to 20 percentage points worse than Doherty amplifiers. As a consequence, the average efficiency of both the Doherty and outphasing amplifier tends to be similar for large PAPR signals. To overcome this problem, mixed-mode or optimal input drive control has been proposed in the literature [27].

4.2 Outphasing Amplifier with Mixed-Signal Approach

The efficiency of the outphasing amplifier in Fig. 9 is close to the theoretical limit of 78.5% at back-off level less than 10 dB. However, at back-off levels of 10 dB or more, the efficiency drops below that of the Doherty amplifier. At back-off levels of 13 dB or more, the efficiency drops below that of the class-B amplifier. There is also a problem with the dynamic range of the amplitude of $s(n)$. As shown in Eq. (7), $|s(n)| = 2v_{\max}\cos(\phi(n))$. This means that $\phi(n)$ must be controlled with high precision in order to accurately create amplitude values close to zero. Nevertheless, the phase imbalance between the two branch amplifiers inhibits the high-precision control of $\phi(n)$ and makes it difficult to accurately amplify signals with an amplitude close to zero. Digital compensation has been reported as a means of overcome the dynamic range problem [30].

Mixed-mode operation has been reported as a way to solve the dynamic range issues as well as poor efficiency at large output power back-off [27]. In mixed-mode operation, input signals with amplitudes below a certain threshold, v_{th}, are split by the SCS into two constant phase (ϕ_a) signals where amplitude modulation is used to obtain the high precision at small input power levels as shown in Eq. (9) and Eq. (10).

$$\phi(n) = \begin{cases} \arccos\left(\dfrac{|s(n)|}{2v_{\max}}\right) & |s(n)| \geqq v_{\text{th}} \\ \phi_a & |s(n)| < v_{\text{th}} \end{cases} \tag{9}$$

$$v(n) = \begin{cases} v_{\max} & |s(n)| \geqq v_{\text{th}} \\ |s(n)| & |s(n)| < v_{\text{th}} \end{cases} \tag{10}$$

4.3 Analysis and Design of the DOPA

Figure 10 shows the block diagram of the proposed dual-input DOPA where branch amplifiers of an outphasing amplifier are replaced with Doherty amplifiers. The Doherty amplifiers consist of impedance inverters with characteristic impedance Z_C and Z_{2C} while the Chireix combiner is constructed using two transmission lines whose characteristic impedances are Z_1 and Z_2. The impedance inverters have an electrical length of 90 degrees while the Chireix combiner is realized by the series configuration of the Chirex combiner with the electrical length of $90 \pm \Delta$ degrees. It should be noted that this is different from [26] where the impedance inverter of each carrier device also acts as the Chireix combiner. Figure 11 shows the theoretical input drive required to operate the proposed DOPA where Doherty mode is used for small input power levels and outphasing mode is used for large input power levels with the change of operation occurring at point v_{th}.

4.3.1 Chireix Combiner Design Consideration

One condition is placed on the design of the Chireix combiner for ease of analysis and design of the DOPA. Namely, the impedance observed at Z_L and Z_{L2} are purely resistive (R_{L0}) when the DOPA is driven with the constant phase ϕ_a. This condition allows the impedance nodes Z_{LC}, Z_{L2C}, Z_{LP} and Z_{L2P} to be analyzed in the same way as a typical Doherty amplifier. In other words, the constant phase amplitude modulation mode in mixed-mode operation can be replaced with Doherty mode operation.

4.3.2 Load Impedance during Doherty Mode

By designing the Chireix combiner as described earlier, both Z_L and Z_{L2} become R_{L0} Ohms during the Doherty mode. The drain voltage of all devices is assumed to be the same in this paper. The characteristic impedances Z_C and Z_{2C} are set to $2R_{L0}$ Ohms and electrical lengths θ_C and θ_{2C} are set to 90 degrees. The impedance nodes Z_{LC}, Z_{L2C}, Z_{LP} and Z_{L2P}

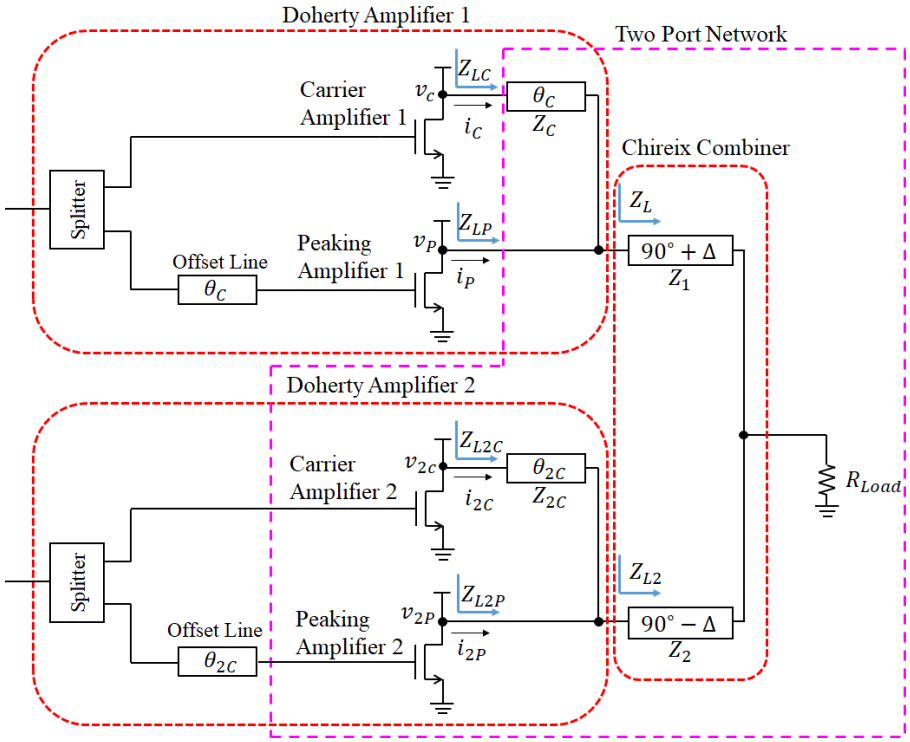

Fig. 10 Block diagram of the proposed DOPA

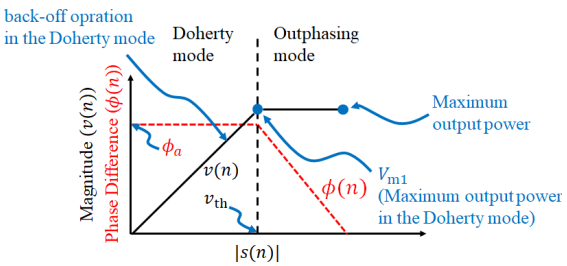

Fig. 11 Operation modes for the DOPA

are analyzed as in a typical symmetrical Doherty amplifier as follows.

$$Z_{LC} = Z_{L2C} = \begin{cases} 4R_{L0} & P_O = P_{\mathrm{m1}} - 6(\mathrm{dB}) \\ 2R_{L0} & P_O = P_{\mathrm{m1}}(\mathrm{dB}) \end{cases} \tag{11}$$

$$Z_{LP} = Z_{L2P} = \begin{cases} \infty & P_O = P_{\mathrm{m1}} - 6(\mathrm{dB}) \\ 2R_{L0} & P_O = P_{\mathrm{m1}}(\mathrm{dB}) \end{cases} \tag{12}$$

where P_{m1} is the maximum output power during the Doherty mode and P_O is the instantaneous output power of the DOPA.

4.3.3 Load Impedance during Outphasing Mode

All the devices are assumed to operate at saturation in the outphasing mode. The impedance nodes Z_{LC}, Z_{L2C}, Z_{LP} and Z_{L2P} are determined by analyzing the two-port network shown in Fig. 10. By analyzing the two-port network using ABCD matrix notation [25], [29], the impedance nodes Z_{LC}, Z_{L2C}, Z_{LP} and Z_{L2P} during the outphasing mode can be expressed as

$$Z_{LC} = Z_C \tag{13}$$

$$Z_{L2C} = Z_{2C} \tag{14}$$

$$Z_{LP} = \frac{Z_C Z_L}{Z_C - Z_L} \tag{15}$$

$$Z_{L2P} = \frac{Z_{2C} Z_{L2}}{Z_{2C} - Z_{L2}}. \tag{16}$$

From Eq. (13) to Eq. (16), it is apparent that as the outphasing angle ϕ tends towards 0 degree, the impedances Z_L and Z_{L2} will become smaller [28]. In addition, the impedance presented to the peaking amplifiers Z_{LP} and Z_{L2P} also decrease while the impedance observed by the carrier amplifiers Z_{LC} and Z_{L2C} remain constant.

This might seem counterintuitive but the behavior of Z_{LC} and Z_{L2C} during the outphasing mode can be explained as follows. Since all the devices in the DOPA operate as voltage sources with a magnitude of V_M, the voltage at the combining node of the Doherty combiner is fixed as $V_c = V_M e^{j(\phi(n)-\pi/2)} = -jV_M e^{j\phi(n)}$, where $\pi/2$ is due to the phase offset realized at the input network of the peaking amplifier. The 90-degree transmission line of the Doherty combiner converts V_c into a current from the device as $V_M e^{j\phi(n)}/Z_C$ for the Doherty amplifier 1 and $V_M e^{j\phi(n)}/Z_{2C}$ for the Doherty amplifier 2. Therefore, Z_{LC} and Z_{L2C} can be determined as Z_C and Z_{2C} respectively by using Ohm's law. Any type of DPA can therefore be designed and connected to a Chireix combiner assuming that the initial impedance presented by the Chireix combiner satisfies Doherty operation.

This feature is very important in the design to bring out the best performance of the devices. In the outphasing mode, the load impedance moves only for the peaking amplifier. To utilize this benefit, the device size of both peaking amplifiers are larger than that of the carrier amplifiers. It should be noted that the load impedance of the peaking amplifier at P_{m1} is higher than the optimum load impedance of the device for the peaking amplifiers.

4.3.4 Combiner Design and Efficiency Comparison

An example Chireix combiner that can be cascaded with two Doherty combiners can be realized using the previous analysis as follows: $Z_C = Z_{2C}$ set to 50 Ohms, $\theta_C = \theta_{2C}$ set to 90 degrees, $Z_1 = Z_2$ set to 25 Ohms, R_{Load} set to 12.5 Ohms and $\Delta = 60$ degrees. Using this Chireix combiner, Z_L and Z_{L2} are both 25 Ohms for $\phi(n) = \phi_a = 60$ degrees. It should be noted that this is an example combiner and that the design parameters ought to be tuned to fit the target devices.

For ease of explanation, only impedance trajectories for Z_{LC} and Z_{LP} are shown in Fig. 12 and Fig. 13, respectively. Both Z_{LC} and Z_{L2C} move from 100 Ohms to 50 Ohms during Doherty operation, while it remains constant during outphasing operation. Z_{LP} and Z_{L2P} move from an open to 50 Ohms during the Doherty mode and move towards $5.7 - j2.8$ Ohms and $5.7 + j2.8$ Ohms respectively during the outphasing mode. In this design, when the drain supply voltage is equal for both the carrier and peaking amplifier, the maximum output power ratio can be calculated from the ratio between Z_{LC} and Z_{LP}, which in this case is 1:7. Therefore, a device size ratio of 1:7 utilizes the entire dynamic load modulation range during the outphasing mode. The theoretical efficiency profile is plotted and compared to the aforementioned amplifier topologies in Fig. 9. For the example DOPA, the first efficiency peak is located at 12 dB output power back-off with almost no drop in efficiency between the first efficiency peak and the efficiency at output power saturation. This is unlike the 1:3 asymmetrical Doherty amplifier, which also has its first efficiency peak located at 12 dB output power back-off but suffers from a large drop in efficiency between the first and second efficiency peak. Note that reducing the device size of the peaking amplifier in this design narrows the power range where high efficiency can be obtained.

4.4 Measurement Result

The harmonically-tuned dual-input DOPA was developed with two 10 W GaN HEMTs (CGH40010F) for the carrier amplifiers and two 45 W GaN HEMTs (CGH40045F) for the peaking amplifiers. Note that the combination of devices used limits the extension of output power in outphasing mode to approximately 4.7 dB ($\approx 10\log_{10}(6/2)$), instead of 6 dB as discussed in Sect. 4.3.4.

MEGTRON6 R-5775 from Panasonic is used as the substrate for the DOPA. The two Doherty amplifiers had the same design and were designed using a general PA design

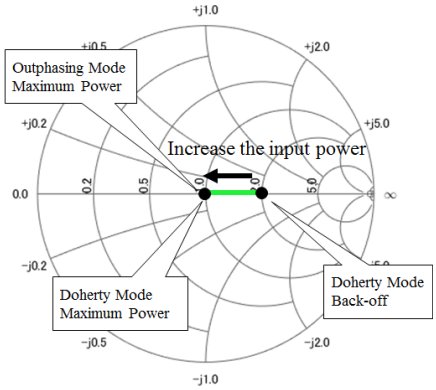

Fig. 12 Impedance trajectory of the carrier amplifier during both the Doherty mode and the outphasing mode with a normalized impedance of 50 Ohms

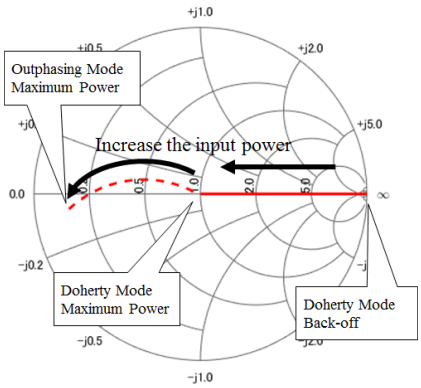

Fig. 13 Impedance trajectory of the peaking amplifier during both the Doherty mode and the outphasing mode with a normalized impedance of 50 Ohms

method including harmonic impedance termination. The splitter for the Doherty amplifier was a Wilkinson splitter with a splitting ratio of 1:2. The target frequency is 622 MHz, which is LTE Band 71, because of the operating frequency of the driver amplifiers. However, as there are fabrication tolerances, the operating frequency shifted down to 580 MHz. The drain voltages of all devices are set to 28 V with the carrier and peaking device of each branch biased in class-AB and class-C, respectively. The simulated CW drain efficiency and power added efficiency (PAE) with input-signal-control are shown in Fig. 14. Given that the DOPA is a dual-input architecture, the total input power for calculating PAE is the summation of the two input power values, which is $P_{in} = P_{in1} + P_{in2}$, where P_{in1} is the input power to the Doherty amplifier 1 and P_{in2} is the input power to the Doherty amplifier 2.

The input signal profile of the DOPA is shown in Fig. 11. The output power corresponding to v_{th} is 4.7 dB backed-off from the maximum output power level. In the simulation, the maximum output power is 51.8 dBm and the peak efficiency reaches 80% thanks to the manipulation of harmonic impedances. The efficiency even at 15 dB back-off is 72%. The photograph of the measurement setup with

the developed DOPA is shown in Fig. 15. Additionally, the block diagram of the measurement setup is shown in Fig. 16. The signal generator has two output ports that are phase coherent. The output signal of the DOPA is fed back to the signal generator for DPD estimation. For the CW measurements both the input power and the phase difference between the two Doherty amplifiers are controlled with the results shown in Fig. 14. The maximum output power is 51.2 dBm. The measured peak drain efficiency is 77.7% at 50.2 dBm output power. The measured drain efficiency at 15 dB back-off is 61.4%. The performance when using a modulated signal is also verified. For modulated performance, 10 MHz LTE signals with various PAPRs are used to confirm the efficiency potential at different back-off levels.

The output spectrum of the DOPA with a memory digital pre-distorter (DPD) is shown in Fig. 17. The average output power is 40.8 dBm with a modulated drain efficiency of 70.2%. This is equivalent to 10.4 dB back-off which is our definition of PAPR for linearized modulated results. Figure 18 shows the drain efficiency, PAE and gain with respect to the average output power of the DOPA. A summary of the adjacent channel leakage ratio (ACLR) performance using three 10 MHz LTE signals with different PAPR is shown in Table 1. The ACLR at 10.4 dB output power back-off is better than −47.7 dBc, which is acceptable for practical use. In addition, the EVM was 0.8%. Please note that the parameters of the DPD were not optimally tuned. It is expected that by optimizing the DPD parameters, the ACLR and EVM performance of the DOPA can be further enhanced. A sum-

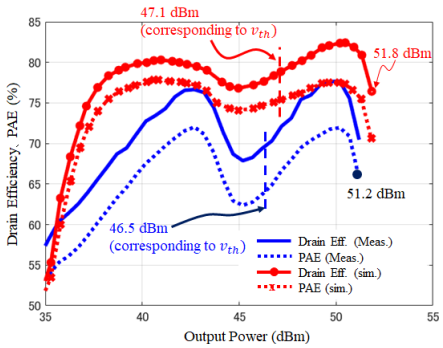

Fig. 14 Simulation and measurement results of the CW efficiency with respect to the output power level

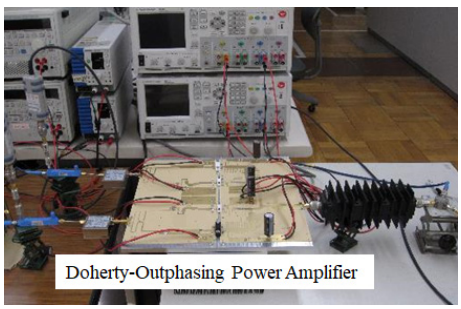

Fig. 15 Photograph of the measurement setup including the dual-input DOPA

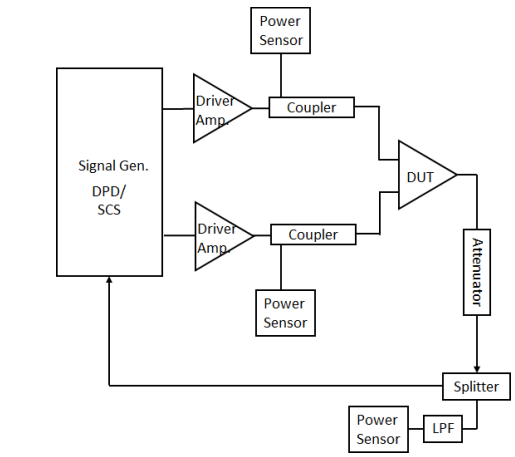

Fig. 16 Block diagram of the measurement setup

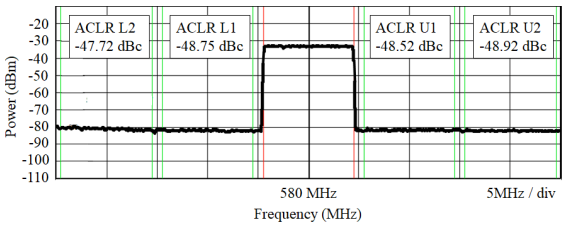

Fig. 17 Output spectrum of the DOPA after linearization

Table 1 Measured ACLR using three 10 MHz LTE signals with different PAPR

Back-off dB	Pout dBm	ACLR dBc
9.1	42.1	−47.6
10.4	40.8	−48.5
11.9	39.3	−50.3

Table 2 Performance summary and comparison with other highly-efficient PA architectures

	Freq. GHz	Architecture	Device	Back-off dB	Drain Eff. %	Pout dBm	Signal
[14]	2.14	Envelope Tracking	GaAs HVHBT	7.7	60	45.2	WCDMA 5MHz
[7]	3.5	2-way Doherty	GaN HEMT	9	58	N/A	LTE 20MHz
[7]	3.5	2-way Doherty	GaN HEMT	9.7	56	N/A	LTE 20MHz × 5
[24]	2.14	4-way Outphasing	N/A	9.2	55.6	41.5	WCDMA 5MHz
[10]	2.14	3-way Doherty	GaN HEMT	11.5	55	38.5	LTE 5MHz
This Work	0.58	Doherty-Outphasing	GaN HEMT	10.4	70.2	40.8	LTE 10MHz
This Work	0.58	Doherty-Outphasing	GaN HEMT	11.9	66.6	39.3	LTE 10MHz

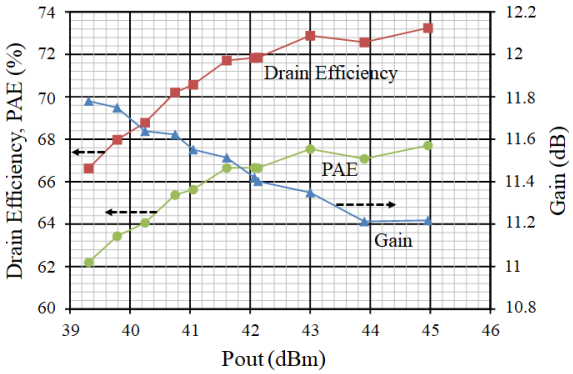

Fig. 18 Measured drain efficiency, PAE and gain versus average output power using 10 MHz LTE signals with various PAPRs

mary of the modulated signal measurements as well as a comparison to other three or more device architectures using a modulated signal is shown in Table 2. Even at the back-off level of 11.9 dB, a modulated efficiency of 66.6% was measured. Regarding the use of wider bandwidth signals in the order of 100's MHz, as the bandwidth of the output signals of the SCS are wider than the original signal, further set-up modifications are required to analyze the performance potential.

5. Conclusion

A highly efficient DOPA was developed and evaluated using OFDM signals with a PAPR of 10 dB or more. Although the proposed DOPA requires multiple-inputs and an increase in design costs, the efficiency of the DOPA outperformed the reported modulated efficiency, attaining 70.2% modulated efficiency for a 10 MHz OFDM signal with a PAPR of 10.4 dB. This demonstrates the feasibility of multiple-input amplifiers and shows that they are a potential solution to improve the modulated efficiency in response to the ever increasing modulation order of future wireless systems.

References

[1] Center for Low Carbon Society Strategy, Japan Science and Technology Agency, "Impact of progress of information society on energy consumption (vol.1)," March 2019.

[2] Ministry of Internal Affairs and Communiocations, Japan, "Beyond 5g promotion strategy," June 2020.

[3] V.K. Bhargava and A. Leon-Garcia, "Green cellular networks: A survey, some research issues and challenges," 2012 26th Biennial Symposium on Communications (QBSC), pp.1–2, 2012.

[4] The Government of Japan, "The long-term strategy under the paris agreement," June 2019.

[5] W.H. Doherty, "A new high efficiency power amplifier for modulated waves," Proceedings of the Institute of Radio Engineers, vol.24, no.9, pp.1163–1182, 1936.

[6] F.H. Raab, "Efficiency of doherty rf power-amplifier systems," IEEE Transactions on Broadcasting, vol.BC-33, no.3, pp.77–83, 1987.

[7] M. Özen and C. Fager, "Symmetrical Doherty Amplifier with High Efficiency over Large Output Power Dynamic Range," 2014 IEEE MTT-S International Microwave Symposium (IMS2014), pp.1–4, June 2014.

[8] T. Yamamoto, T. Kitahara, and S. Hiura, "50% drain efficiency doherty amplifier with optimized power range for w-cdma signal," 2007 IEEE/MTT-S International Microwave Symposium, pp.1263–1266, 2007.

[9] T. Kitahara, T. Yamamoto, and S. Hiura, "Asymmetrical doherty amplifier using gan hemts for high-power applications," 2012 IEEE Topical Conference on Power Amplifiers for Wireless and Radio Applications, pp.57–60, 2012.

[10] M.J. Pelk, W.C.E. Neo, J.R. Gajadharsing, R.S. Pengelly, and L.C.N. de Vreede, "A high-efficiency 100-W GaN three-way Doherty amplifier for base station applications," IEEE Transactions on Microwave Theory and Techniques, vol.56, no.7, pp.1582–1591, July 2008.

[11] A. Barthwal, K. Rawat, and S.K. Koul, "A design strategy for bandwidth enhancement in three-stage doherty power amplifier with extended dynamic range," IEEE Transactions on Microwave Theory and Techniques, vol.66, no.2, pp.1024–1033, 2018.

[12] A. Grebennikov, "High-efficiency advanced multistage doherty gan hemt power amplifiers," RF Technology International, vol.1, pp.10–18, 02 2012.

[13] M.J. Roberts, "Understanding the 3 level doherty," 2016 46th European Microwave Conference (EuMC), pp.1357–1361, 2016.

[14] J. Jeong, D.F. Kimball, M. Kwak, C. Hsia, P. Draxler, and P.M. Asbeck, "Modeling and design of rf amplifiers for envelope tracking wcdma base-station applications," IEEE Transactions on Microwave Theory and Techniques, vol.57, no.9, pp.2148–2159, Sept. 2009.

[15] L.R. Kahn, "Single-sideband transmission by envelope elimination and restoration," Proceedings of the IRE, vol.40, no.7, pp.803–806, 1952.

[16] F.H. Raab, "High-efficiency linear amplification by dynamic load modulation," IEEE MTT-S International Microwave Symposium Digest, 2003, vol.3, pp.1717–1720, 2003.

[17] C. Sánchez-Pérez, M. Özen, C.M. Andersson, D. Kuylenstierna, N. Rorsman, and C. Fager, "Optimized design of a dual-band power amplifier with sic varactor-based dynamic load modulation," IEEE Transactions on Microwave Theory and Techniques, vol.63, no.8, pp.2579–2588, 2015.

[18] K. Mimis, G.T. Watkins, A. Yamaoka, and K. Yamaguchi, "Output harmonic optimisation of dynamically load modulated power amplifiers," 2016 46th European Microwave Conference (EuMC), pp.1071–1074, 2016.

[19] H. Cao, J. Qureshi, T. Eriksson, C. Fager, and L. de Vreede, "Digital predistortion for dual-input doherty amplifiers," 2012 IEEE Topical Conference on Power Amplifiers for Wireless and Radio Applications, pp.45–48, 2012.

[20] H. Chireix, "High power outphasing modulation," Proceedings of the Institute of Radio Engineers, vol.23, no.11, pp.1370–1392, 1935.

[21] M. Özen, M. van der Heijden, M. Acar, R. Jos, and C. Fager, "A generalized combiner synthesis technique for class-E outphasing transmitters," IEEE Trans. Circuits Syst. I, vol.64, no.5, pp.1126–1139, May 2017.

[22] P.E. de Falco, P. Pednekar, K. Mimis, S.B. Smida, G. Watkins, K. Morris, and T.W. Barton, "Load modulation of harmonically tuned amplifiers and application to outphasing systems," IEEE Trans. Microw. Theory Techn., vol.65, no.10, pp.3596–3612, Oct. 2017.

[23] S. Kimura, K. Tamanoi, T. Maniwa, T. Takano, "Efficiency improvement of transmitter for mobile phone base station using outphasing amplifier," in IEICE Technical Report, vol.113, no.260, MW2013-109, pp.53–58, Oct. 2013.

[24] T.W. Barton and D.J. Perreault, "Four-way microstrip-based power combining for microwave outphasing power amplifiers," IEEE Transactions on Circuits and Systems I: Regular Papers, vol.61, no.10, pp.2987–2998, Oct. 2014.

[25] A. Yamaoka, T.M. Hone, and K. Yamaguchi, "70 % efficient dual-input doherty-outphasing power amplifier for large papr signals," 2019 IEEE MTT-S International Microwave Symposium (IMS), pp.556–559, June 2019.

[26] A.R. Qureshi, M. Acar, J. Qureshi, R. Wesson, and L.C.N. de

Vreede, "A 112W GaN dual input Doherty-outphasing power amplifier," 2016 IEEE MTT-S International Microwave Symposium (IMS), pp.1–4, May 2016.
[27] J.H. Qureshi, M.J. Pelk, M. Marchetti, W.C.E. Neo, J.R. Gajadharsing, M.P. van der Heijden, and L.C.N. de Vreede, "A 90-W peak power GaN outphasing amplifier with optimum input signal conditioning," IEEE Transactions on Microwave Theory and Techniques, vol.57, no.8, pp.1925–1935, Aug. 2009.
[28] S.C. Cripps, *RF Power Amplifiers for Wireless Communications*, 2nd ed. Norwood, MA: Artech House Microwave Library, 2006.
[29] A. Yamaoka, T. Hone, K. Yamaguchi, "Dual input Doherty-Outphasing power amplifier," The IEICE Transactions on Electronics (Japanese Edition), vol.J103-C, pp.488–495.
[30] T. Hwang, K. Azadet, R.S. Wilson, and J. Lin, "Linearization and imbalance correction techniques for broadband outphasing power amplifiers," IEEE Transactions on Microwave Theory and Techniques, vol.63, no.7, pp.2185–2198, 2015.

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