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A Brief History of Nyquist Analog-to-Digital Converters

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SUMMARY This paper reviews and discusses a brief history of Nyquist ADCs. Bipolar flash ADCs for early development stage of HDTV and digital oscilloscopes, a Bi-CMOS two-step flash ADC using resistive interpolation for home HDTV receivers, a CMOS two-step flash ADC using capacitive interpolation for handy camcorders, pipelined ADCs using CMOS operational amplifiers, CMOS flash ADCs using dynamic comparator and digital offset compensation, SAR ADCs using low noise dynamic comparators and MOM capacitors, and hybrid ADCs are reviewed.

key words: *ADC, flash ADC, two-step flash ADC, pipelined ADC, SAR ADC*

1. Introduction

The last 50 years has been an era where analog equipment has been replaced by digital devices. The digitalization of devices and systems is due to the technological shift from bipolar to CMOS, the development of logic circuits and memory circuits owing to scaling laws. Also, the developments of data converters such as ADCs and DACs were indispensable. In this paper, I would like to describe a brief history of ADC development that contributed to the realization of these digital electronic devices. Since it is difficult to cover all of them, the paper will describe the transition in the circuit and architecture of Nyquist ADCs, each conversion rate is equal to the sampling rate, including the relation to the electronic devices in which they were used.

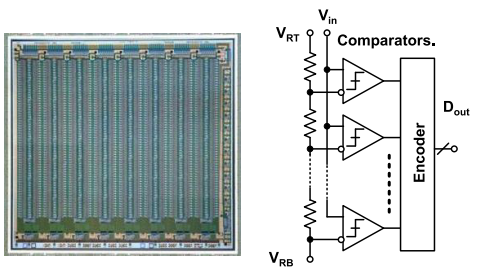
2. Bipolar Flash ADC

Research and development of the digitization of TV systems began in the latter half of the `1970s, but the integrated circuit of ADC had not progressed.

An 8-bit ADC for video systems was developed by TRW and 10-bit ADC was commercialized by ADI equipped with various hybrid ICs, as shown in Fig. 1 and there was no monolithic integrated 10-bit ADC for video. In addition, this ADC board was priced at about 1 million yen and consumed 20 W, so it could not be used for industrial use, as well as consumer use.

We started developing ADC for video at Panasonic, and in 1981 we developed a video-rate 8-bit ADC [1], and in 1982 we developed a video-rate 10-bit ADC shown in Fig. 2 (a) [2]. At that time, the CMOS technology required for S/H circuits could not be used, so a flash type which required many comparators shown in Fig. 2 (b) was used. A comparator using an ECL circuit is shown in Fig. 3. The S/H function is realized by fixing the comparison result of the latch at the clock edge. Since the power consumption of the ECL circuit is proportional to the number of current sources, the power consumption is reduced to 1/3 of the conventional bipolar flash ADC by stacking it vertically instead

Fig. 1 10-bit ADC board (ADI).



(a) 10-bit flash ADC (b) Flash ADC architecture

Fig. 2 10-bit flash ADC and it's ADC architecture.

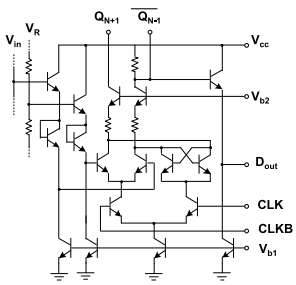


Fig. 3 Bipolar comparator.

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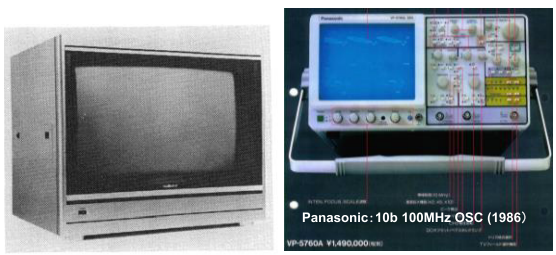
of horizontally cascade connections as in conventional ECL.

The mismatch voltage of the transistors constituting the ADC comparator requires a standard deviation of about 0.1 mV for a 10-bit resolution. The accuracy was achieved by using a high-precision bipolar transistor developed for low power consumption and high integration of IC for analog signal processing circuits in VHS video-tape recorders.

This ADC was used for digital video switchers and HDTV relay equipment at the Seoul Olympics in 1988. Figure 4 (a) shows the MUSE HDTV receiver at that time. The HDTV requires A/D conversion of 25 MHz wideband video signals from a camera and requires a conversion speed of 75 MS/s or more, but at that time such a high-speed ADC did not exist. In 1984, we developed an 8-bit 120 MS/s ADC [3]. Bipolar technology with trench isolation was used for higher speed and lower power. This ADC was also used in the early digital oscilloscopes shown in Fig. 4 (b). Later, in 1991, a 6-bit 1 GS/s ADC was developed [4] and was installed in an 8-bit 1 GS/s digital oscilloscope.

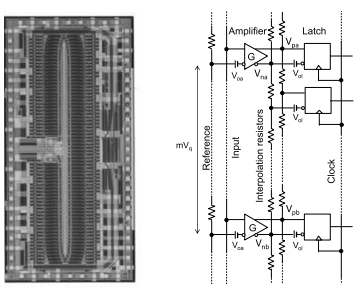
In 1994, we developed a 10-bit 300 MS/s ADC [5], which was realized by introducing interpolation technique into the flash ADC, as shown in Fig. 5 (a), and achieved 4 times higher conversion speed compared to other high-speed 10-bit ADCs. In contrast to the conventional flash architecture, that uses one pre-amplifier for 8 latch circuits shown in Fig. 5 (b), and 8 series-connected load resistors are used between the outputs of one pair of pre-amplifiers to reduce the DNL to about 1/8. This ADC was used for optical transmission systems for HDTV signals.

Bipolar flash ADCs are rarely used today. This is because the power consumption and chip area are inherently large, and it is difficult to achieve high accuracy. However, due to the minimum conversion latency, flash ADCs using CMOS technology are still used today at low resolutions of 6-bit or less. CMOS flash ADCs will be described in Sect. 6. At the dawn of digital TV development in the `1980s, CMOS technology was not available, so bipolar flash ADCs supported the development of the HDTV systems.



(a) MUSE HDTV receiver (b) Digital oscilloscope

Fig. 4 HDTV receiver and digital oscilloscope.



(a) 10-bit 300MS/s ADC (b) Parallel interpolation

Fig. 5 10-bit 300MS/s ADC and parallel interpolation.

3. Bi-CMOS Two-Step Flash ADC

A fundamental issue of flash ADC is that the circuit size and power consumption increase exponentially with respect to resolution. For every one bit of resolution increase, the circuit size and power consumption are doubled. Therefore, as shown in Fig. 6, if the conversion is performed in two steps, the circuit size and power consumption are greatly reduced. When ADC with N bit resolution is converted in the upper M bits, the number of comparators n is

$$n = 2^M + 2^{N-M}. \tag{1}$$

For example, when N = 10 and M = 5, the number of comparators n decreases to 1/16 from 1024 in flash ADC to 64 in two-step ADC. The actual lower conversion takes an overlap structure, so it is about 1.5 times larger than this, but it still decreases to about 1/10.

The major problem is that the input signal voltage should not change in the two conversion periods, so an S/H circuit is required. In bipolar transistors, since the base current flows, the voltage changes with time, making it difficult to achieve high-precision S/H. In the latter half of the `1980s, Bi-CMOS technology, which combines bipolar transistors and MOS transistors, became available, so in 1991 we developed a two-step flash 10-bit ADC using Bi-CMOS technology shown in Fig. 7 (a) [6].

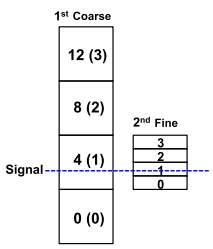
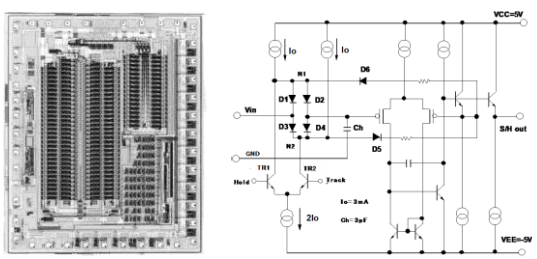


Fig. 6 Two-step A/D conversion.



(a) Bi-CMOS two-step ADC (b) Bi-CMOS S/H

Fig. 7 Bi-CMOS two-step flash ADC and Sample/Hold.

Figure 7 (b) shows an S/H circuit. High-precision S/H was realized by preventing leakage current from the S/H capacitor using a PMOS-input operational amplifier. In addition, in this S/H circuit, a diode bridge is used instead of a conventional CMOS switch to suppress the dependence of the ON-resistance of the switch on the input voltage. For this reason, a good distortion of −80 dB was achieved. Another problem with two-step flash ADC is the deterioration of linearity due to the mismatch between the coarse and fine conversion. The situation is shown in Fig. 8. When the fine conversion range is wider than the conversion range of the coarse unit, the voltage range for which a specific conversion value becomes narrow, and in some cases, a miscode that is no output is likely to occur. If it is narrow, the voltage range for which a specific conversion value is taken becomes wider, and in both cases, the conversion error increases. Therefore, as shown in Fig. 9, we devised an A/D conversion by interpolation in which the differential output ends of two differential amplifiers selected by the coarse conversion are connected by a series of resistor strings and the voltages between the taps are compared. As shown in Fig. 10 (a), the conventional conversion method uses a fixed reference voltage, so if there is a mismatch between the two conversion ranges, the DNL of the specific conversion value deteriorates. On the other hand, the conversion using interpolation shown in Fig. 10 (b) has a conversion that flexibly responds to mismatches as if using a spring, and the DNL of the specific conversion output is not degraded and the error is dispersed, so smooth A/D conversion characteristics can be realized.

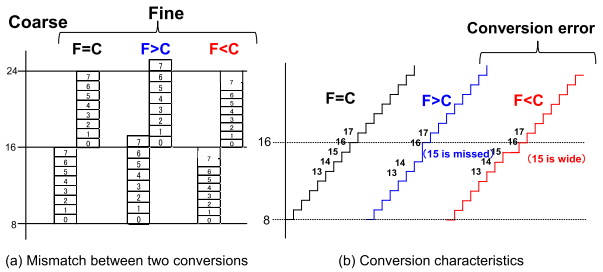


Fig. 8 Linearity issue of the two-step flash ADC.

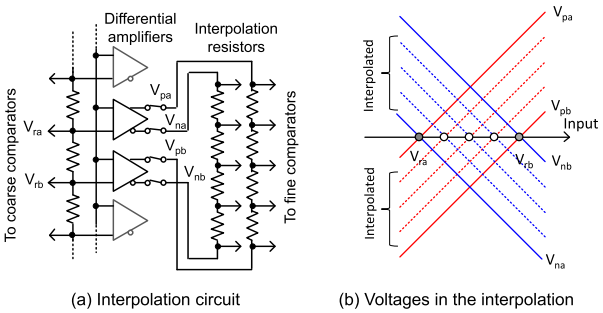


Fig. 9 Interpolation circuit and voltages.

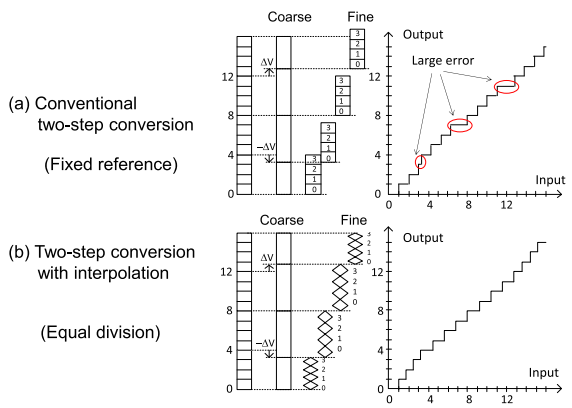


Fig. 10 Conversion error in conventional and interpolated two-step conversion.

This ADC was used in a home HDTV receiver for which Japan manufacturers shared the responsibility to develop the necessary integrated circuits for the HDTV test broadcast in 1989. However, since Bi-CMOS was a transitional technology and was later unified with CMOS, the basic idea of this A/D conversion method was used in CMOS technology.

4. CMOS Two-Step Flash ADC

Handheld camcorders, which record and play back video images on tape, became popular before digital cameras. The first hit was the TR55 released by SONY in 1989. It uses 8 mm cassette videotape. In response, Panasonic released the NV-S1, a handy camcorder using digital signal processing in 1990. The successor and signal processing block diagram are shown in Fig. 11 [7]. The use of digital signal processing technology makes it easier to realize automatic white balance and automatic focus functions, but the biggest motivation for using digital signal processing technology is image stabilization.

Handy camcorders are required to be small and lightweight, which means that camera shake is likely to occur, which has a vital impact on image quality. Therefore, as shown in Fig. 12, the image is recorded in the frame memory once and the motion vector is detected. At this time, it is necessary to judge whether the movement is due to the subject or the camera shake. Therefore, several observation areas are provided, and if the correlation of movement in each observation area is small, it is judged to be movement caused by the subject, and if the correlation is large, it is due

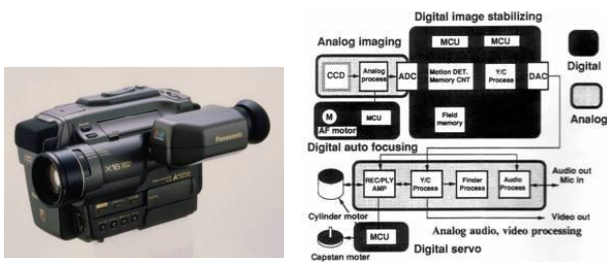


Fig. 11 Handy camcorder using digital signal processing and it's block diagram.

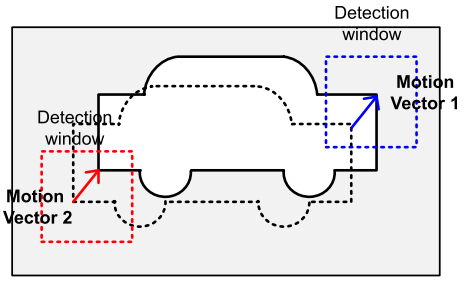
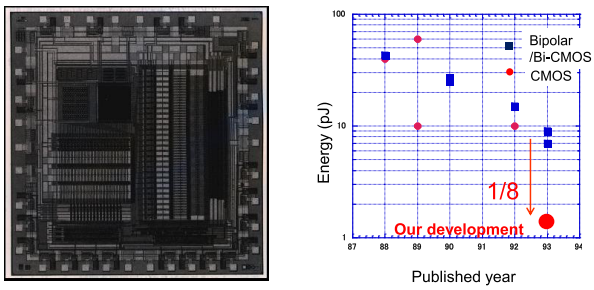
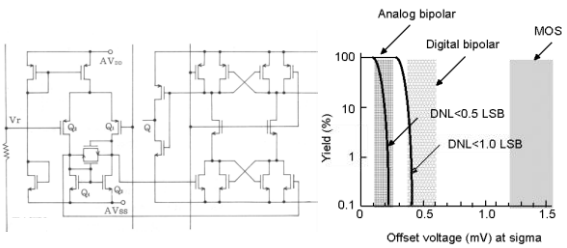


Fig. 12 Motion detection.



(a) CMOS 10-bit 20MS/s 30mW ADC (b) Conversion energy of video-rate 10-bit ADC

Fig. 13 CMOS two-step flash ADC and conversion energy.



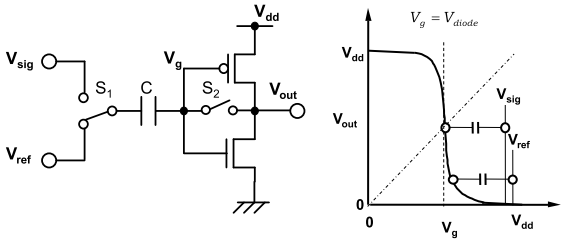
(a) CMOS comparator (b) Offset voltage at sigma

Fig. 14 CMOS comparator and offset voltage at sigma.

to camera shake. The image shake is corrected by controlling the memory address of the read image by this extracted motion vector due to the camera shake.

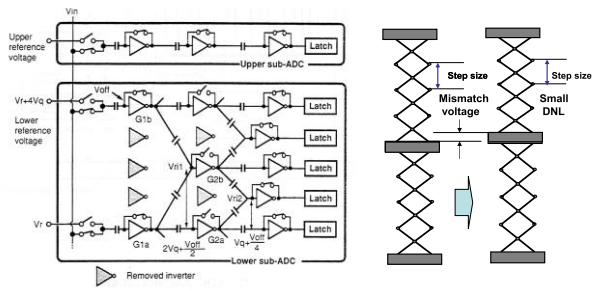
For portable devices, low power consumption is extremely important to extend battery life and to reduce the temperature rise when miniaturized. A low-power video-rate 10-bit ADC was required for the image signal processing, but the power consumption of ADC at that time was higher than 200 mW, which was unacceptable to be used in portable devices. In addition, CMOS was necessary to reduce cost and size, but CMOS ADC was not necessarily low power, and it was comparable to ADC using bipolar. Therefore, we developed a 10-bit 20 MS/s 30 mW CMOS ADC shown in Fig. 13 (a) in 1993 [8]. Figure 13 (b) shows the energy consumption of video-rate 10-bit ADCs at around `1990. Compared to bipolar ADC, CMOS ADC was not necessarily low power, but the energy consumption of this CMOS ADC attained 1/8 that of other ADCs. Low energy consumption has been realized.

Figure 14 (a) shows the CMOS comparator at that



(a) Chopper inverter comparator (b) I/O characteristics

Fig. 15 Chopper inverter comparator and I/O characteristics.



(a) CMOS comparator with capacitive interpolation (b) Conversion image

Fig. 16 CMOS comparator with capacitive interpolation and conversion image.

time [9]. It was a CMOS replacement of the transistor of a bipolar comparator. Figure 14 (b) shows a comparison of mismatch accuracy, while the standard deviation of the bipolar comparator is 0.3 mV or less, MOS is about four times larger at 1.2 mV. In addition, in the case of MOS transistor, the size dependency is large, and a considerably large size MOS transistor is required, so the speed deteriorates, and the power consumption increases. Therefore, in this ADC, the chopper inverter proposed by Dingwall shown in Fig. 15 (a) [10] was used as a comparator. It is composed of elements and circuits suitable for CMOS, such as inverters, switches, and capacitors. As shown in Fig. 15 (b), it can absorb and cancel the mismatch voltage of the circuit, which is an issue of CMOS circuits. High accuracy comparison and S/H function are realized, so a two-step flash ADC can be configured. In addition, the parasitic capacitance can be reduced by shrinking the area of the circuit to reduce the power consumption.

However, the accuracy was about 8-bits as it was [11], so further ingenuity was added. Figure 16 (a) shows upper coarse and lower fine comparator circuits. In the lower fine comparators, the outputs of the first stage inverters were combined by capacitance in units of four, and the outputs of the next stage inverters were combined by capacitance in units of two.

By performing interpolation using the capacitance in this way, as shown in Fig. 16 (b), the mismatch can be effectively suppressed to 1/4, so that it can realize a 10-bit resolution. Furthermore, since the gray inverters can be removed, it is possible to further reduction of power consumption.

Due to this breakthrough in low power operation,

almost all ADCs subsequently used CMOS technology. CMOS benefited from technology scaling, and the fact that it became highly integrated, high speed, and low power. However, this two-step flash ADC did not become a major trend, and the main role of the ADC architecture shifted to the pipelined ADC described below.

5. Pipelined ADC

As shown in Fig. 17, a pipelined ADC amplifies the subtracted signal using a CMOS operational amplifier (OP amp.) by controlling DAC based on the level of the input signal and the next stage samples the output signal and repeats in a pipeline manner. In this process, the output of each conversion stage has a fold characteristic of input and output voltage. Finer folding characteristics can be obtained as the conversion stage progresses. Therefore, to increase the resolution, it is sufficient to increase the conversion stage, so the resolution scalability is higher than that of the two-step flash ADC and it is easy to develop a high-resolution ADC.

However, as shown in Fig. 18 (a), the signal voltage jumps out of the conversion range caused by the offset voltage of the comparator, so the linearity deteriorates.

This problem was fundamentally solved by the redundant configuration shown in Fig. 18 (b) [12]. By making the turning points sufficiently inside of the conversion range, linearity is not affected by the offset voltage of the comparator, so high accuracy is possible, and pipelined ADCs have rapidly spread.

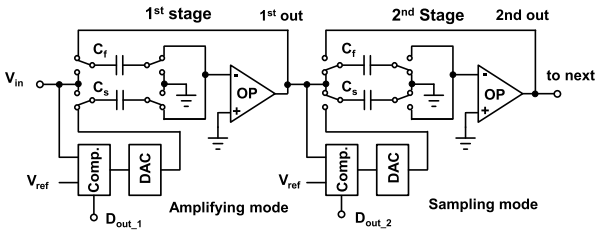


Fig. 17 Pipelined ADC.

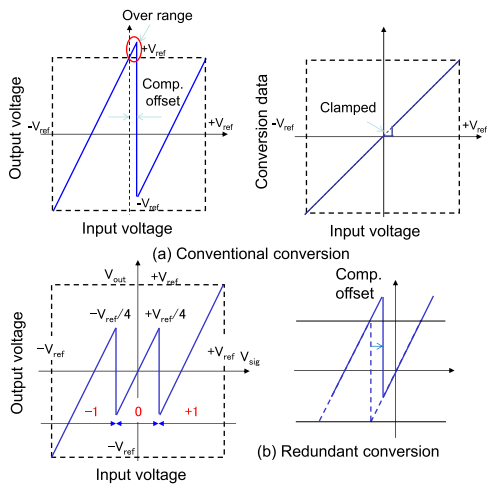


Fig. 18 Conventional folding and conversion erase. and solution by redundancy.

Another important technology is the development of the gain boost circuit shown in Fig. 19 [13]. The required gain G of the OP amp. is expressed as follows with respect to the resolution N.

$$G(dB) > 6N + 10 \tag{2}$$

If the resolution is 14-bits, a gain of 94 dB or more is required. For an OP amp., a single-stage configuration is desirable because the conversion speed deteriorates when using multi-stage configuration, but the gain is about 50 dB, which does not reach the target. Therefore, as shown in Fig. 19, by boosting the gain using amplifiers in the cascode circuit, a gain of 100 dB or more can be achieved with a single-stage configuration.

The other important circuit technology is the bootstrap switch shown in Fig. 20 [14], [15]. A conventional CMOS switch has an input voltage-dependent ON-resistance and causes distortion. The bootstrap switch can realize a constant low ON-resistance over the full input voltage range by keeping constant large V_{GS} and can suppress the distortion of sampled input voltage.

The pipelined ADC has improved its performance with the above circuit technologies and has achieved a conversion speed of about several hundred MS/s with a resolution of about 12-16 bits. The technology scaling of CMOS increased the speed of the OP amp. during the period of popularization, and the availability of high-precision MIM capacitor also supported the development.

The linearity of pipelined ADC is mainly determined by the capacitance mismatch and the lack of gain of the amplifier. The lack of gain can be solved by using a gain boost circuit. The required capacitance mismatch for N bit ADC is

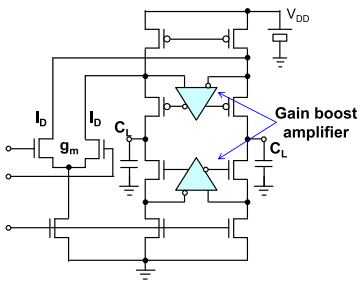
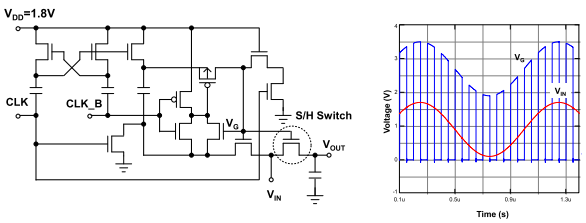


Fig. 19 Gain-boost amplifier.



(a) Bootstrap switch circuit. (b) V_{in} and V_G.

Fig. 20 Bootstrap switch.

$$\frac{\Delta C}{C} < \frac{1}{2^N}. \tag{3}$$

Also, a capacitance mismatch is inversely proportional to the square root of capacitance. If γ is the proportionality coefficient,

$$\frac{\Delta C}{C} = \frac{\gamma}{\sqrt{C}}. \tag{4}$$

Therefore, the capacitance value C should be

$$C > \gamma^2 2^{2N}, \tag{5}$$

and when the resolution increases by one bit, four times larger capacitance is required.

For thermal noise constraints, refer to V_{ref}, k is the Boltzmann constant and T is the absolute temperature, the capacitance C should be satisfied

$$C > 18kT\left(\frac{2^N}{V_{ref}}\right)^2. \tag{6}$$

Therefore, even in this case, if the resolution increases by one bit, four times larger capacitance is required.

Regarding the conversion speed, the gain bandwidth of the amplifier GBW is relative to the conversion speed f_c of ADC.

$$GBW > N \cdot f_c \tag{7}$$

The GBW can be expressed with g_m as the transconductance of the first stage in Fig. 19, C_L is the load capacitance, I_D is the operating current of the first stage, V_{eff} is the effective gate voltage of the MOS transistor in the first stage,

$$GBW = \frac{g_m}{2\pi C_L} = \frac{I_D}{\pi V_{eff} \cdot C_L}. \tag{8}$$

Therefore, the drain current of the MOS transistor in the first stage I_D is as follows

$$I_D > \pi V_{eff} \cdot C_L \cdot N \cdot f_c. \tag{9}$$

If the capacitance is determined from the resolution, the operating current is proportional to the product of the resolution and the conversion frequency. Also, from the stability of the negative feedback circuit, if f_{p2} is the second pole frequency,

$$GBW < \frac{f_{p2}}{2}. \tag{10}$$

Although the condition must be satisfied, the second pole frequency is inversely proportional to the channel length L.

$$f_{p2} \propto \frac{1}{L} \tag{11}$$

Therefore, to increase the conversion frequency f_c, it is necessary to use a fine transistor with a short L. However, since the operating voltage decreases as the transistor becomes finer, there is a limit to the speed of pipelined ADC using an OP amp. In addition, linearity can be significantly improved by digital calibration and error correction, but noise cannot be improved by such techniques. So, if the resolution and reference voltage are given, the required capacitance is determined by Eq. (6), and the required current is determined by Eq. (9). Therefore, it is difficult to improve the ADC performance with technology scaling, and it is not easy to reduce the power consumption of the pipelined ADC at a high conversion frequency. For this reason, the performance of the pipelined ADC using OP amp. is limited, and recently SAR ADC and SAR ADC-based pipelined ADC became mainstream.

6. CMOS Flash ADC

The flash ADC using bipolar transistors has hardly been used since the `2000s, but Flash ADC has a small area with a resolution of 6-bits or less. Since the latency of sampling the input signal and then outputting the conversion value is as short as one clock, it is used not only as a low-resolution ADC but also as a multi-bit quantizer for the pipelined ADCs and the multi-bit ΔΣADCs. The accuracy in flash ADC is mainly determined by the variations in the offset voltage of the comparators.

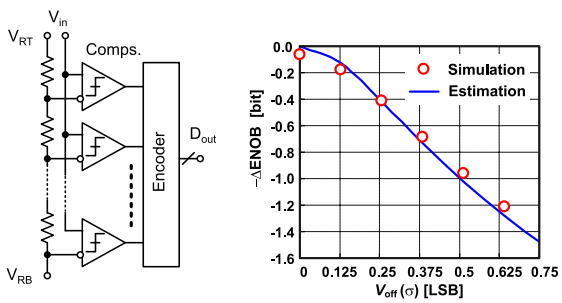
Figure 21 shows the configuration of the flash ADC and the effective bit reduction ΔENOB as a function of the standard deviation of the offset voltage distribution of the comparator normalized by the quantization voltage V_q can be expressed by the following equation $V_{off}(\sigma)$.

$$\Delta ENOB = \frac{1}{2}\log_2\left(1 + 12\left(\frac{V_{off}(\sigma)}{V_q}\right)^2\right) \tag{12}$$

From this equation, it can be seen that if the reduction of the effective bit is 0.5 bits, $V_{off}(\sigma)$ is required about 0.3 V_q. When the transistor size is increased, the offset voltage distribution narrows, but since the area increases and the capacitance increases, another method is required to reduce the offset voltage distribution, if using a small transistor.

A CMOS flash ADC uses a dynamic comparator that does not flow a steady current as shown in Fig. 22 [16].

For comparison, only the polarity of the input differential voltage needs to be judged in synchronized with the clock timing, and a differential flip-flop is fine, but a dynamic amplifier is often placed in the front stage to increase



(a) Flash ADC (b) Offset voltage and reduction of ENOB

Fig. 21 Flash ADC and reduction of ENOB.

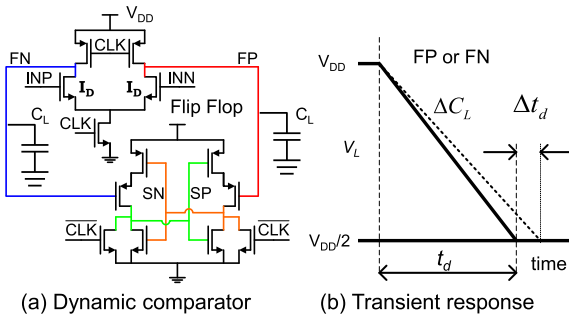


Fig. 22 Dynamic comparator and transient responce.

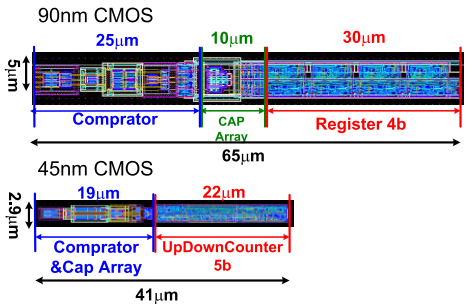


Fig. 23 Layouts of dynamic comparators with offset cancel.

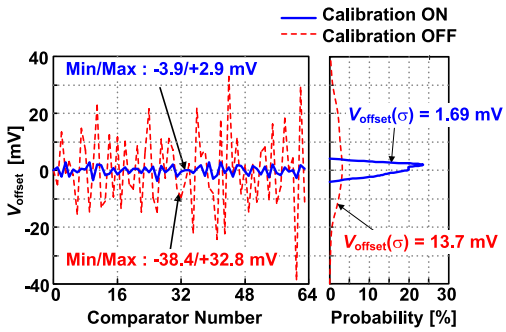


Fig. 24 Offset voltage of dynamic comparator and compensation effect.

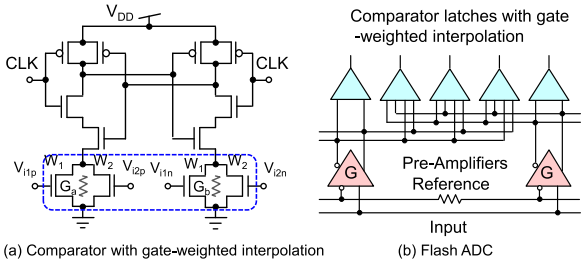


Fig. 25 Comparator with gate-weighted interpolation and flash ADC.

sensitivity.

To compensate for the offset voltage of the comparator, the load capacitance C_L of this dynamic amplifier is often adjusted digitally [17]. The change in delay time t_d when the load capacitance C_L is changed by ΔC_L is

$$\frac{\Delta t_d}{t_d} = \frac{\Delta C_L}{C_L}. \tag{13}$$

Using the transistor's effective gate voltage V_{eff}, the input offset voltage ΔV_{off} is

$$\Delta V_{off} = \frac{V_{eff}}{2}\frac{\Delta C_L}{C_L}. \tag{14}$$

The input offset voltage can be adjusted by adjusting the load capacitance of the dynamic amplifier. Figure 23 shows the layout of the dynamic comparator having an input offset voltage adjustment function when 90 nm CMOS and 45 nm CMOS are used. Since an input offset voltage adjustment circuit is required in addition to a normal comparator circuit, the area increases, but the ratio of the adjustment circuit decreases with technology scaling.

Figure 24 shows the input offset voltages of the comparators when the input offset voltage adjustment is performed and not performed [18]. When the input offset voltage adjustment is not performed, a large offset voltage of 38 mV at the peak and 13.7 mV with a standard deviation are measured, but when the offset voltage is adjusted, 3.9 mV and 1.69 mV are measured respectively. Measured input offset voltage is sufficiently small for a 7-bit flash ADC. To reduce power consumption, a CMOS flash ADC using dynamic comparator with an offset compensation circuit has become popular.

As another circuit technology, interpolation that evenly divides two voltages without power consumption increase can be realized by inserting MOS transistors operating in a linear region at the source side of the flip-flop constituting the comparator, as shown in Fig. 25 [14], [19].

The synthetic conductance G_a and G_b can be described with voltages V_{i1p}, V_{i2p}, V_{i1n}, V_{i2n}

$$\begin{cases} G_a = \dfrac{\mu C_{ox}}{L}\left[W_1(V_{i1p} - V_T) + W_2(V_{i2p} - V_T)\right] \\ G_b = \dfrac{\mu C_{ox}}{L}\left[W_1(V_{i1n} - V_T) + W_2(V_{i2n} - V_T)\right] \end{cases}, \tag{15}$$

where μ is the mobility, C_{ox} is the unit gate capacitance, L is the channel length, W is the channel width, and V_T is the threshold voltage of MOS transistor. Therefore, the difference in conductance is

$$G_a - G_b = \frac{\mu C_{ox}}{L}\left[W_1(V_{i1p} - V_{i1n}) + W_2(V_{i2p} - V_{i2n})\right]. \tag{16}$$

Here, if the ratio of the channel widths W_1 and W_2 are taken below, it is possible to compare the difference voltage divided by m at the k^{th} voltage.

$$W_1 : W_2 = \frac{m-k}{m} : \frac{k}{m} \quad k < m \tag{17}$$

If this comparator is arranged between the outputs of the preceding amplifier of the gain-G as shown in Fig. 25 (b), the offset voltage of the flip flop can be reduced to 1 / G [19]. In this figure, for simplicity, there are 4 flip flops per one amplifier, but actually there are 8 flip flops. This ADC uses a front-stage amplifier through which flows a steady current instead of a dynamic amplifier to suppress kickback noise,

so it does not achieve ultimate low power consumption. But it achieved a low power consumption of 1/10 compared to that of the equivalent ADCs at the time.

7. SAR ADC

A SAR ADC consists of capacitance, switches, a comparator, and logics, and is extremely simple, as shown in Fig. 26 [20], [21]. By making the comparator dynamic, an ADC that does not flow steady current can be realized, so it can be operated with extremely low power consumption. Figure 27 shows the function of capacitance.

In addition to S/H operation using the capacitance, the capacitance can be switched to create the reference voltage required for conversion by connecting the capacitance to the reference voltage or to the ground. Suppose that α of the total capacitance C is connected to the voltage V_{ref}, and the remaining capacitance $(1-\alpha)$ is connected to the ground. Here α takes a value from 0 to 1. The terminal voltage V_x is

$$V_x = -V_{in} + \alpha V_R. \tag{18}$$

Therefore, A/D conversion can be realized by changing the α by switches and converging V_x to zero. Therefore, the SAR ADC can realize the S/H operation and quantization operation which are essential for A/D conversion with a minimum configuration.

Figure 28 shows a typical comparator [18] used in the SAR ADC. The front stage is a dynamic amplifier, and the rear stage is a latch circuit. The transistors marked with ◯ are provided to reduce noise, and the effect will be shown later.

Unlike ordinary amplifiers, the dynamic amplifier in the front stage can realize the amplification action without a steady current flow. The operation is shown in Fig. 29, and the waveforms at the output ends is shown in Fig. 30.

First, as shown in Fig. 29 (a), CLK takes "0", the transistor pair, M_1 and M_2 that converts the input signal voltage difference to output current difference is cut off. The output node voltages become V_{DD}, and the output load capacitances C_L are pre-charged to V_{DD}. Next, as shown in Fig. 29 (b), when CLK takes "1", transistors M_1 and M_2 become active, and the output currents flow through the transistor pair and the voltages at the output end decrease as shown in Fig. 30. At this time, the node with a large drain current drops quickly and the node with a small drain current drops slowly, so that a voltage difference occurs between the output terminals.

If the elapsed time since CLK takes "1" is T_a, the output signal voltage difference ΔV_{out} for the input signal voltage difference ΔV_{in},

$$\Delta V_{out} = -\frac{g_m T_a}{C_L}\Delta V_{in}. \tag{19}$$

If the average voltage of the two output voltages is V_{com} and the average current of the two drain currents is I_{DA}, then T_a is

$$T_a = \frac{C_L(V_{DD} - V_{com})}{I_{DA}}. \tag{20}$$

Thus, the gain G is obtained using the effective gate voltage V_{eff} of transistors M_1 and M_2

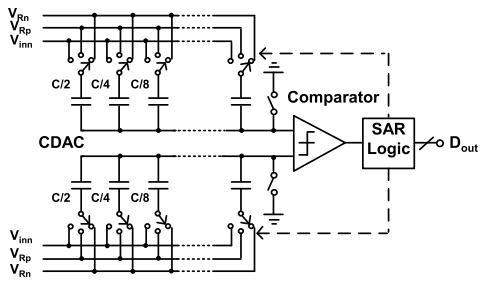


Fig. 26 SAR ADC.

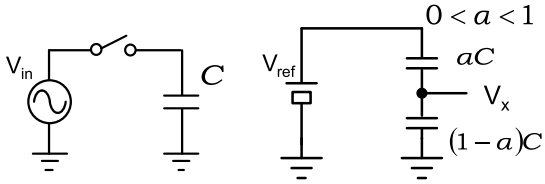


Fig. 27 Function of capacitance.

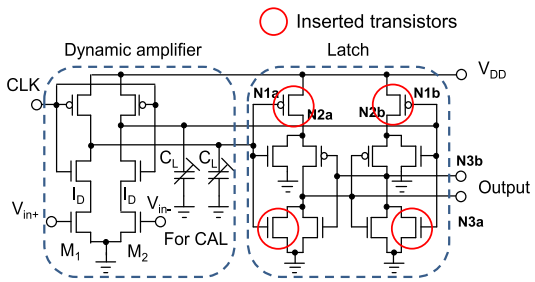


Fig. 28 Low-noise dynamic comparator.

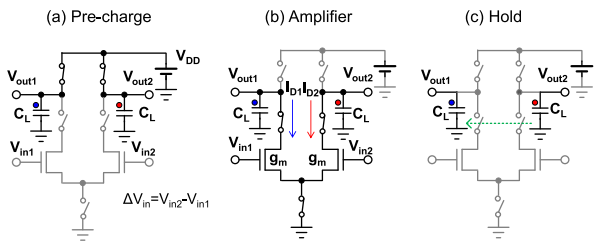


Fig. 29 Operation of the dynamic amplifier.

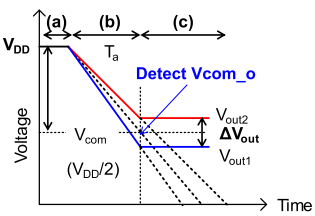
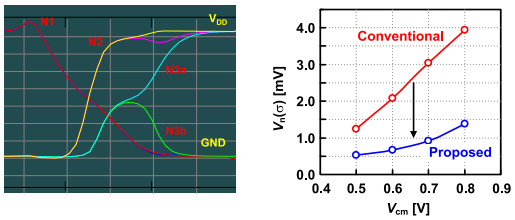


Fig. 30 Transition of node voltages in the dynamic amplifier.



(a) Waveforms in dynamic comparator (b) Noise voltages

Fig. 31 Waveforms and noise in the dynamic comparator.

$$G = \frac{2(V_{DD} - V_{com})}{V_{eff}}. \tag{21}$$

For example, if V_{DD} = 1.2 V, V_{com} = $V_{DD}/2$ = 0.6 V, and V_{eff} = 0.15 V, the gain G is about 8, so a sufficiently large gain can be obtained at the front stage.

When used as a front stage of a dynamic comparator, the latch circuit starts a positive feedback operation near the intermediate voltage of the power supply voltage, so the output voltage may drop as it is. But when used as an amplifier, as shown in Fig. 29 (c), the common voltage V_{com} of the output signal is detected to cutoff the transistor M_1 and M_2, the output voltage can be held as shown in Fig. 30 [22]. By using this dynamic amplifier, pipelined ADCs and ΔΣADCs can be realized.

Figure 31 (a) shows the voltage-waveforms in the dynamic comparator shown in Fig. 28. When CLK becomes "1" and current flows through transistors M_1 and M_2, the output node voltages of the previous dynamic amplifier drop. As the voltage drops, current flows through the inserted PMOS transistors, and the NMOS transistors are cut off, so the voltage at node N2 rises. Accordingly, when node N3 rises, the positive feedback circuit is activated, and one node becomes V_{DD} and the other node becomes GND depending on the input voltage difference and the comparison ends.

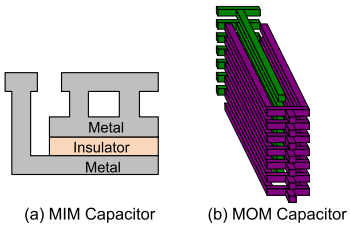
Figure 31 (b) shows the noise voltage of the comparator with respect to the input common voltage V_{cm} when a conventional latch circuit is used and when a transistor marked with ◯ is inserted. It can be seen that the noise voltage can be lowered by about 1/3 of the conventional latch circuit by inserting the transistors marked with ◯ [18]. Since the CMOS amplifier is placed in front of the noisy latch circuit by the insertion transistor, it is considered that the input-referred noise is reduced.

In SAR ADCs, since malfunctions occur during SAR operation due to comparator noise and the effective resolution of the ADC deteriorates, SAR ADCs with higher resolution can be realized by using this low-noise comparator.

The noise voltage v_n of the dynamic comparator determined by the dynamic amplifier of the previous stage, when the noise generated from the subsequent latch circuit is sufficiently suppressed, is given below [23].

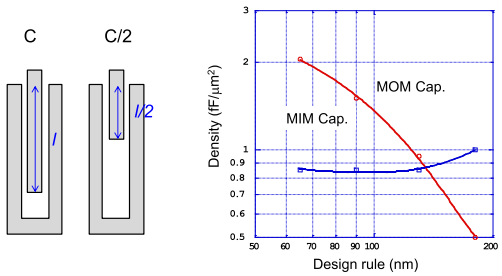
$$v_n \approx \sqrt{\frac{2kT}{C_L}\frac{V_{eff}}{V_{DD}}} \tag{22}$$

Therefore, in a high-resolution SAR ADC that requires low noise, the load capacitance C_L increases. Therefore, the power consumption increases and the operating speed decreases.



(a) MIM Capacitor (b) MOM Capacitor

Fig. 32 MIM capacitor and MOM capacitor.



(a) Capacitance adjustment (b) Capacitance density

Fig. 33 Capacitance adjustment and capacitance density.

Incidentally, changes in the capacitance formation method have greatly contributed to the progress of SAR ADCs.

Pipelined ADCs require high-precision capacitance of several pF, and MIM capacitance is used in which the insulating film is sandwiched between the upper and the lower metals shown in Fig. 32 (a), while SAR ADCs use MOM capacitance that uses the lateral capacitance between the wires shown in Fig. 32 (b).

SAR ADCs require not the same capacitance, but a reduced capacitance with each ratio of 1/2. For example, a 10-bit SAR ADC with a total capacitance of 1 pF would ideally require a minimum capacitance of about 2 fF, which is 1/512. Such a small capacitance can be realized by, for example, adjusting the wiring length as shown in Fig. 33 (a). By this method, a small capacitance of about 40 aF can be realized empirically. As shown in Fig. 33 (b), the MOM capacitor has a feature that the capacitance density increases according to the miniaturization of the process. For this reason, if the capacitance value is the same, the distance between the wires is reduced according to the miniaturization of the process. Furthermore, the wiring is multi-layered and the number of metal layers is increased, the occupied area of the capacitor is reduced with the progress of process technology. This contributes to an increase in conversion speed and a decrease in conversion energy consumption in SAR ADC.

Figure 34 shows the capacitance configuration of a SAR ADC with a resolution of 12-bit. By using split capacitance, the capacitance ratio can be suppressed, so there is no need to use a very small capacitance. However, It causes

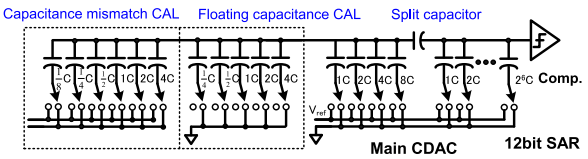


Fig. 34 Capacitor banks in 12-bit SAR ADC.

the problem that linearity deteriorates due to the influence of parasitic capacitance. This can be addressed by controlling the floating capacitance. In addition, the MOM capacitor has a larger mismatch than the MIM capacitor, but this can also be addressed by using the mismatch compensation capacitance. In other words, capacitance issues can be addressed by capacitance [24], [25].

In addition, the conventional problem of SAR ADC is that it requires the higher operating frequency of SAR, which is N times higher than the conversion frequency, where N is the resolution bit. It can be solved by self-clocking technology that creates an operating clock. One method to form a self-clock is using the operating characteristics of the dynamic comparator shown in Fig. 28. As shown in Fig. 31 (a), in a dynamic comparator, both outputs are in the same logical state during comparison, and the comparison outputs take a different logical state when determined, so the state of the comparator can be detected using exclusive OR, and when the comparison is confirmed, the next operating clock can be generated automatically.

Conventionally, SAR ADC has been considered unsuitable for high-speed conversion due to its low conversion frequency. It is true that the conversion speed of a single SAR ADC is slower than that of a flash ADC, but as shown in Fig. 26, it has the simplest configuration as a function of ADC: capacitances, switches, a comparator, and logics, and the capacitance value is mainly determined by kT/C noise. Therefore, a large capacitance is required for high resolution, for example, about 2 pF is required for 12-bits, but only 5 fF is enough for 8-bits. Since a small capacitance can be used, it is possible to significantly reduce the area of the capacitor and the size of the switch. In the case of low resolution, the speed and energy consumption are mainly determined by the logic circuits, so the benefits of technology scaling can be fully enjoyed. Since it does not use an OP amp., it can be operated at low voltage, so it is suitable for scaled technology. Therefore, recently, an ultra-high-speed ADC of which conversion speed of 64 GS/s has been developed by using 256 interleaving SAR ADCs as shown in Fig. 35 [26], and it is used in DSP for optical communication and PAM4 for wire lines.

SAR ADC is expected to continue to be the mainstream of Nyquist ADC because it can be further shrunken, lower-energy, and faster by benefiting from further technology scaling. But it is difficult to increase resolution more in SAR ADC alone. The output voltage of the CDAC after the A/D conversion finishes, becomes a residual voltage about the quantization voltage and this voltage can be used for the input of a ΔΣADC or the input of a pipelined ADC, as shown

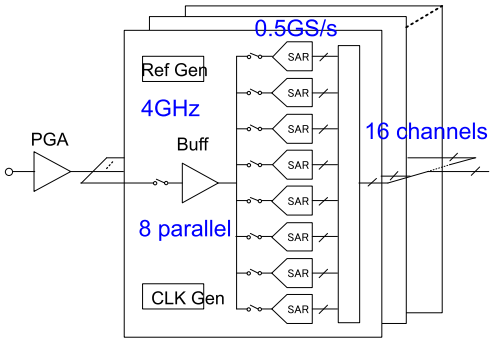


Fig. 35 64 GS/s interleaved SAR ADC.

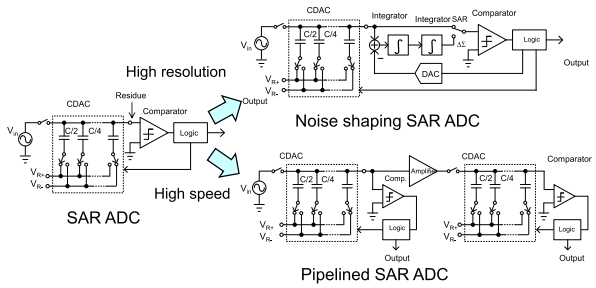


Fig. 36 SAR ADC based hybrid ADCs.

in Fig. 36.

These ADCs are called hybrid ADC and become booming. Noise shaping SAR ADCs have been developed to increase the resolution being higher than 12-bit [27]–[29]. Also, pipelined SAR ADCs have been developed to increase the conversion speed without interleaving [30], [31].

8. Important Works for Future ADCs

Lastly, I would like to introduce two important works for future ADCs. One is the continuous ADC that does not use the sample and hold (S/H) circuit at the input terminal. The S/H circuit causes a large rush current at the switching timing and results in difficulty of ADC peripherals such as anti-alias filters and input and reference voltage buffers. The power consumption increases, and the transient response is degraded.

A continuous-time pipelined ADC shown in Fig. 37 that does not sample the input signal has attractive feature [32], [33]. The delay time of the subtract signal at the input node of the CT filter is compensated by the delay line. The input node of the ADC is not capacitive but resistive and the rush current does not exist.

Other important work is kT/C noise cancellation. The essential challenge in ADC is to overcome kT/C noise. High-resolution ADC needs large capacitance, which increases the conversion energy and degrades the conversion speed. This has long been thought to be unavoidable, but recently research has begun to overcome this problem [34]. Two capacitances and switches, and an amplifier were used to reduce the influence of kT/C noise by changing the po-

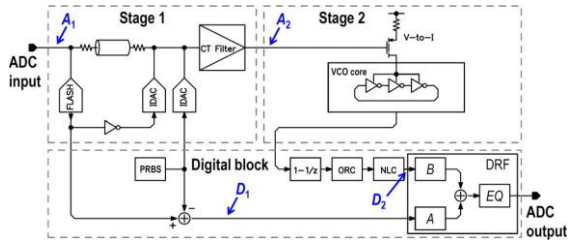


Fig. 37 continuous-time pipelined ADC.

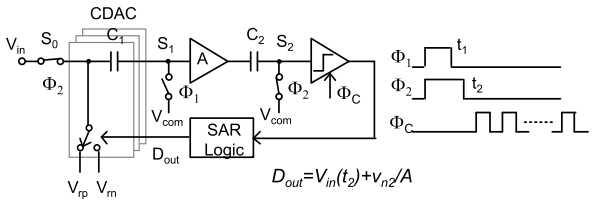


Fig. 38 SAR ADC with kT/C Noise cancellation.

sition and timing of signal sampling, as shown in Fig. 38. Firstly, the switch S_1 is opened at t_1 and signal $V_{in}(t_1)$ is sampled in C_1 and kT/C noise is caused. Next, the switch S_0 and S_2 are opened at t_2 and the input voltage of the amplifier is

$$V_{in}(t_2) - V_{in}(t_1) - v_{ns1} - V_{os}, \tag{23}$$

where v_{ns1} is the kT/C noise in C_1 and V_{os} is the offset voltage of the amplifier. The stored voltage in C_2 is

$$A[V_{in}(t_2) - V_{in}(t_1) - v_{ns1} - V_{os}] + v_{ns2}, \tag{24}$$

where A is the gain of the amplifier and v_{ns2} is the kT/C noise in C_2. When D_{out} is applied to the input terminal, The input voltage of the amplifier is

$$D_{out} - V_{in}(t_1) - v_{ns1} - V_{os}, \tag{25}$$

and the input voltage of the comparator is

$$A[D_{out} - V_{in}(t_2)] + v_{ns2}. \tag{26}$$

Thus

$$D_{out} = V_{in}(t_2) + v_{ns2}/A. \tag{27}$$

Therefore, if gain A is high enough, the kT/C noise in C_2 can be suppressed sufficiently. This method demonstrates that we have a solution to conquer the kT/C noise issue.

9. Conclusions

A brief history of the developments in Nyquist ADCs, which deal with wideband signals such as video signals has been reviewed. Around `1980, when starting the development of digital TV, a 10-bit ADC that could convert TV signals was at the board level using many ICs. It was extremely expensive and impractical. For this reason, in 1982, we developed a monolithic IC of video-rate 10-bit ADC, but CMOS was not widespread and hadn't sufficient accuracy at that time. It was a flash type using bipolar technology that could be highly accurate and high-speed, so it was possible to convert at an ultra-high-speed conversion of about 1 GS/s, and it was used in early digital oscilloscopes. However, the number of comparators increases exponentially with respect to the resolution, and the area and power consumption increase significantly, so there are limits to cost, power consumption, and resolution in the flash ADC.

From the latter half of the `1980s, the Bi-CMOS technology became available, and the two-step flash ADC could be realized because the sample and hold circuit could be used. However, since the comparator itself uses bipolar technology, a steady current flows, and there are limits to low power consumption and cost reduction in the two-step flash ADC. In the `1990s, CMOS process became generally available. It was expected to realize an ADC using CMOS for integration with logic circuits, low power consumption, and low cost, but an accuracy of CMOS was not high enough. Therefore, a CMOS video-rate 10-bit ADC using chopper inverter comparator and interpolation technique using capacitance were developed and it realized low power consumption at 1/8 of the previous video-rate 10-bit ADCs. After that, the bipolar ADC that had been used until then was discontinued, and almost all ADCs use CMOS technology. From the latter half of `1990s, A pipelined ADC using CMOS OP amp. became mainstream. This is because the resolution is scalable, and the ADC performance is determined by the CMOS OP amp. In addition, the performance of the CMOS OP amp. was improved because the miniaturization of CMOS was progressing at that time, and the power supply voltage was not too low. The performance of the pipelined ADC was improved. In the `2010s, a SAR ADC dominated. The main reasons are that the power supply voltage has dropped to the point where it becomes difficult to design the CMOS OP amp. due to technology scaling. It is difficult to significantly reduce the operating current of the OP amp.

A SAR ADC consists of capacitance, switches, a comparator, and logics, and is extremely simple. While the capacitance value of the SAR ADC is determined by kT/C noise and does not directly benefit from technology scaling, but by using a dynamic comparator that does not allow steady current to flow, the energy consumption and conversion speed are mainly determined by the logic circuits, and the scaled technology can be used to achieve higher speed and lower energy. This is because it can cope with low voltage operation. The adoption of MOM capacitance using wiring also encouraged its popularization.

Since the SAR ADC has a small capacitance at a low resolution of 8-bits or less, it can achieve an ultra-high-speed conversion by interleaving operation, but it is not easy to achieve a high-resolution and high-speed ADC by interleaving operation. In the future, it is expected that the emphasis will be on hybrid ADC that combines a SAR ADC with a ΔΣADC or a pipelined ADC.

The important works for future ADCs are CT ADC that can avoid the S/H circuit that causes large rush current and

make the design of peripheral circuits, such as anti-alias filters and input and reference voltage buffers, difficult. The CT ADC can avoid the input S/H circuit by using the signal delay element. Other important work is kT/C noise cancellation. The essential challenge in ADC is to overcome kT/C noise. This has long been thought to be unavoidable, but recently the research has begun to overcome this problem. Two capacitances and switches, and an amplifier were used to reduce the influence of kT/C noise by changing the position and timing of signal sampling.

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