

Reduced Peripheral Leakage Current in Pin Photodetectors of Ge on n⁺-Si by P⁺ Implantation to Compensate Surface Holes

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SUMMARY A reduced dark leakage current, without degrading the near-infrared responsivity, is reported for a vertical pin structure of Ge photodiodes (PDs) on n⁺-Si substrate, which usually shows a leakage current higher than PDs on p⁺-Si. The peripheral/surface leakage, the dominant leakage in PDs on n⁺-Si, is significantly suppressed by globally implanting P⁺ in the i-Si cap layer protecting the fragile surface of i-Ge epitaxial layer before locally implanting B⁺/BF₂⁺ for the top p⁺ region of the pin junction. The P⁺ implantation compensates free holes unintentionally induced due to the Fermi level pinning at the surface/interface of Ge. By preventing the hole conduction from the periphery to the top p⁺ region under a negative/reverse bias, a reduction in the leakage current of PDs on n⁺-Si is realized.

key words: *Ge epitaxial layer, near-infrared photodetector, Si photonics, peripheral leakage current*

1. Introduction

A near-infrared (NIR) photodiode (PD) using a Ge epitaxial layer on Si (or Si-on-insulator, SOI) is one of the fundamental building blocks in Si photonics [1]. Ge exhibits a substantial optical absorption coefficient ($>1000\text{ cm}^{-1}$) at the NIR optical communication wavelengths (1.3–1.6 μm) as well as the good compatibility with the Si CMOS process. A vertical pin structure of Ge PD has been integrated with a Si optical waveguide on an SOI wafer for the on-chip optical communication [2]–[7], although a lateral pin structure has recently attracted interests regarding ultrahigh frequency response over 50 GHz [8], [9] to enhance the communication capacity. The vertical pin structure also plays a significant role in free-space/normal-incidence PD arrays required in applications such as multicore-fiber communications [10] and NIR sensing including the eye-safe light detection and ranging (LiDAR) [11]. In vertical pin PDs, an n⁺-Ge/i-Ge/p⁺-Si structure (PD on p⁺-Si) has been commonly used because of the dark leakage current lower than that in an inversely ordered structure of p⁺-Ge/i-Ge/n⁺-Si (PD on n⁺-Si) [12], [13]. However, the inverted configuration of PD on n⁺-Si is convenient for the connection to the next stage circuit such as a transimpedance amplifier, which is usually designed to receive a positive photocurrent from the p contact. As previously reported by the authors [14], the higher leakage current

in the PDs on n⁺-Si is ascribed to the peripheral/surface leakage, rather than the leakage due to the thermal generation of carriers via gap defects of threading dislocations in the i-Ge layer on Si, which is dominant in the PDs on p⁺-Si [15]. The peripheral leakage in the PDs on n⁺-Si is probably derived from free holes [14] unintentionally induced due to the Fermi level pinning at the surface/interface of Ge [16], [17]. These holes induce an electrical conduction from the periphery to the top p⁺ region of the PD on n⁺-Si under a negative/reverse bias, whereas such a conduction is suppressed in the case of the PDs on p⁺-Si because of the top n⁺ region electrically isolated from the peripheral holes via a pn junction. One way to suppress the peripheral leakage in the PDs on n⁺-Si is to use a mesa structure [14], while the footprint of the photodetection area is reduced because inclined {113} facet sidewalls surround a Ge mesa on (001) Si by a selective growth [1].

In this work, a reduction in the leakage current of non-mesa/planar Ge PDs on n⁺-Si is realized by a P⁺ implantation globally in the i-Si cap layer on the i-Ge epitaxial layer before locally forming the top p⁺ region of the pin junction. The peripheral holes are compensated, leading to a reduced leakage current comparable to PDs on p⁺-Si.

2. Holes Induced at Ge Surface/Interface

To verify the presence of free holes at the Ge surface/interface, the Hall effect measurements were performed for Ge epitaxial layers grown by ultrahigh-vacuum chemical vapor deposition (UHV-CVD) with 9%-GeH₄/Ar as a source gas. Here, an undoped Ge layer of 500 nm in thickness was prepared on a 6-inch bonded SOI wafer having a 250-nm-thick top (001) p-Si layer (approximately 10 $\Omega\text{ cm}$) and a 3- μm -thick buried SiO₂ layer. As in previous studies [13]–[15], a low/high temperature two-step growth was carried out to obtain a Ge layer uniform in thickness, i.e., a buffer layer (~50 nm) of elemental Ge was grown at a low temperature of 370°C, followed by a growth at an elevated temperature of 600°C. After the growth, the wafer was cut into pieces, and several different thicknesses of Ge were prepared by a wet etching in a H₂O₂ solution. All samples showed the p-type conduction, independent of the thickness, and the sheet resistances were as low as 20 k Ω /sq., which is approximately one order of magnitude lower than 400 k Ω /sq. for the top Si layer of the SOI substrate. Thus, the observed p-type conduction is ascribed to holes in Ge.

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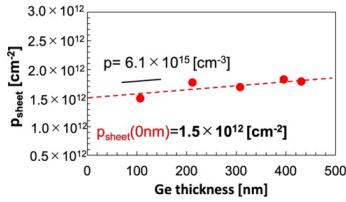


Fig. 1 Sheet hole densities of the Ge epitaxial layer as a function of the Ge thickness.

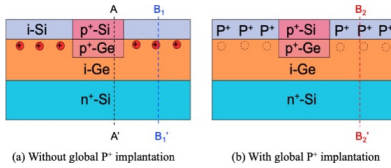


Fig. 2 Schematic cross-sections of PDs. (a) PD without the global P^+ implantation and (b) PD with the global P^+ implantation to compensate the free holes at the Ge surface.

Figure 1 shows the sheet hole density as a function of the Ge thickness. The hole density slightly decreased with decreasing the Ge thickness. The slope, or the hole density per unit volume in the undoped Ge layer was estimated as low as $6 \times 10^{15} \text{ cm}^{-3}$. More importantly, there is an offset in the sheet hole density at the Ge thickness of 0 nm, which is approximately $1.5 \times 10^{12} \text{ cm}^{-2}$. This indicates the presence of free holes at the top Ge surface and/or bottom Ge/Si interface, although the densities cannot be divided between the top surface and bottom interface.

The peripheral leakage in the PDs on n^+ -Si is attributed to the holes at the top Ge surface [14], as shown in Fig. 2 (a). These holes easily induce a leakage current from the periphery to the top p^+ region of the PD under a negative/reverse bias. Typical calculated energy band diagrams along the lines A-A' and B₁-B₁' of Fig. 2 (a) are shown in Figs. 3 (a) and 3 (b), respectively. Here, the bandgap narrowing of a few 10 meV in Ge was ignored, which is induced by the tensile in-plane lattice strain of about 0.2% in Ge due to the thermal expansion mismatch with the Si substrate [1], [14], [15]. Similar to the main part of p^+ -Si/ p^+ -Ge/ i -Ge/ n^+ -Si PD in Fig. 3 (a), the diagram at the periphery in Fig. 3 (b) shows that the Fermi level is located near the valence band maximum of Ge at the top i -Si/ i -Ge interface in the presence of the interface holes with the sheet density of $2.0 \times 10^{12} \text{ cm}^{-2}$. It is mentioned that the holes at the bottom interface are compensated with electrons in the n^+ -Si substrate, i.e., there is no significant difference in the band diagram at around the bottom interface between the presence and absence of the interface holes, as shown in Fig. 3 (b).

To suppress the peripheral leakage by the free holes at the top i -Si/ i -Ge interface, an implantation of P^+ in a Si cap layer on Ge should be effective to compensate the holes, as shown in Fig. 2 (b). The band diagram along the line B₂-B₂' of Fig. 2 (b) is shown in Fig. 3 (c). Here, a uniform P^+ density of $2.0 \times 10^{17} \text{ cm}^{-3}$ was assumed in the top n -Si layer of 120 nm in thickness. This corresponds to the

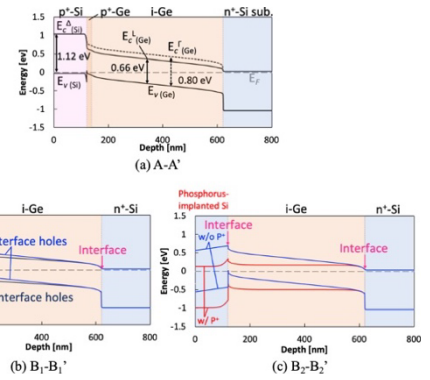


Fig. 3 Calculated energy band diagrams for (a) the main part of p^+ -Si (120 nm)/ p^+ -Ge (20 nm)/ i -Ge (480 nm)/ n^+ -Si PD (along the line A-A' in Fig. 2 (a)), (b) the i -Si/ i -Ge/ n^+ -Si structure comparing the presence and absence of the holes at the top and bottom interfaces with the sheet density of $2 \times 10^{12} \text{ cm}^{-2}$ (along the line B₁-B₁' in Fig. 2 (a)), and (c) the n -Si (P^+ implanted)/ i -Ge/ n^+ -Si structure (along the line B₂-B₂' in Fig. 2 (b)) compared with the i -Si/ i -Ge/ n^+ -Si structure. A uniform P^+ density of $2.0 \times 10^{17} \text{ cm}^{-3}$ in the top Si layer was assumed in (c).

sheet P^+ density of $2.4 \times 10^{12} \text{ cm}^{-2}$, almost equal to the interface hole density of $2.0 \times 10^{12} \text{ cm}^{-2}$. In contrast to the absence of the P^+ implantation, the Fermi level is not located near the valence band maximum of Ge but located near the midgap. This indicates the compensation of the interface holes, potentially preventing the peripheral leakage.

3. PD Preparation

Ge PDs on n^+ -Si were prepared as follows. As the starting substrate, an Sb-doped n^+ -Si (001) wafer was used, whose resistivity was 0.008–0.020 $\Omega \text{ cm}$. First, an undoped Ge epitaxial layer of 500 nm in thickness was grown on n^+ -Si by UHV-CVD. The growth condition was exactly the same as that for the Hall effect measurements in the previous section. Subsequently, a Si cap layer of 120 nm in thickness was grown at 600°C for protecting the fragile surface of Ge using a source gas of 10%-Si₂H₆/Ar. A post-growth annealing was performed at 800°C for 10 min in N₂ to reduce the threading dislocation density in Ge [15].

To compensate holes at the Ge surface (Si cap/Ge interface), a P^+ implantation was performed in the Si cap layer over the entire surface, or globally. Based on the Hall effect measurements, a dose of $2.0 \times 10^{12} \text{ cm}^{-2}$ was used, although a different dose of $4.0 \times 10^{12} \text{ cm}^{-2}$ was also used for comparison. The acceleration voltage was 35 kV, leading to the P^+ distribution mostly in the Si cap layer, as simulated in Fig. 4. Then, to form a vertical pin junction, an implantation of B⁺ and BF₂⁺ was performed locally with resist masks. The B⁺ and BF₂⁺ were implanted at 10 kV with doses of $2.0 \times 10^{14} \text{ cm}^{-2}$ and $1.0 \times 10^{14} \text{ cm}^{-2}$, respectively. As shown in Fig. 4, because of the difference in the penetration depth, the B⁺ ions were implanted across the Si cap/Ge interface to form the p region in the Ge layer, while the BF₂⁺ ions were distributed near the surface of the Si cap layer, realizing a low resistance with a metal contact. The implanted area, cor-

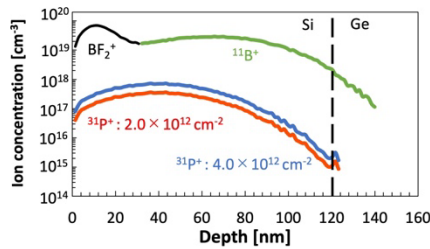


Fig. 4 Simulated distributions of P^+ , B^+ and BF_2^+ ions.

responding to the junction/PD area, was square-shaped with different widths W of 20–500 μm . An activation annealing was performed at 600°C for 5 min in N_2 . Finally, metal electrodes of Al/Ti (with an illumination window opening) were formed. In addition to the PDs on n^+ -Si, Ge PDs on p^+ -Si were prepared as references.

Current-voltage (I-V) characteristics were measured at room temperature (RT) under dark to investigate the leakage current. I-V curves under a light illumination of 1.23 mW at 1550 nm were also measured. Furthermore, responsivity spectra were obtained at 1455–1640 nm.

4. Results and Discussion

Figure 5 shows typical I-V characteristics at RT for PDs on n^+ -Si with and without the P^+ implantation together with a reference PD on p^+ -Si. The width of the squared-shaped PD was 200 μm . Rectifying diode properties were obtained, although the reverse leakage current was different between the PDs. It is important that the P^+ implantation in the Si cap layer of the PDs on n^+ -Si successfully reduced the dark leakage current. The lower dose of $2.0 \times 10^{12} \text{ cm}^{-2}$ more efficiently reduced the leakage current, which was comparable to that in the PD on p^+ -Si.

To examine the leakage mechanism, I-V characteristics for different PD widths were obtained. A typical width dependence is shown in Fig. 6 (a) for the PDs on n^+ -Si with the P^+ implantation dose of $2.0 \times 10^{12} \text{ cm}^{-2}$. The reverse leakage decreased with decreasing the PD width. In Fig. 6 (b), the leakage current at the reverse voltage of 1 V was plotted as a function of the width W . The leakage current I should be composed of peripheral and areal components, and is expressed in the case of the square-shaped PD as

$$I = J_{\text{periphery}}4W + J_{\text{area}}W^2, \quad (1)$$

where $J_{\text{periphery}}$ and J_{area} correspond to the peripheral leakage current per unit length and the one per unit area, respectively. In the logarithmic plot of Fig. 6 (b), the slope of 2 corresponds to the leakage current dominated by the area of the pin junction, whereas the slope of 1 corresponds to the leakage current dominated by the peripheral length. For the reference PDs on p^+ -Si, the slope was almost equal to 2, indicating that the leakage current is dominated by the areal leakage. As in the previous report [15], the areal leakage is derived from the thermal generation of carriers via gap defects of threading dislocations in the i-Ge layer.

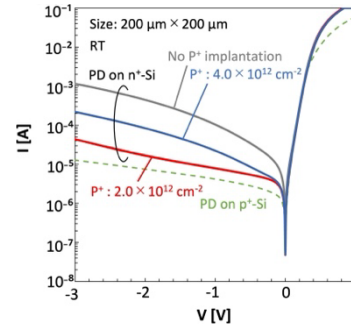


Fig. 5 Typical I-V characteristics of the fabricated Ge PDs.

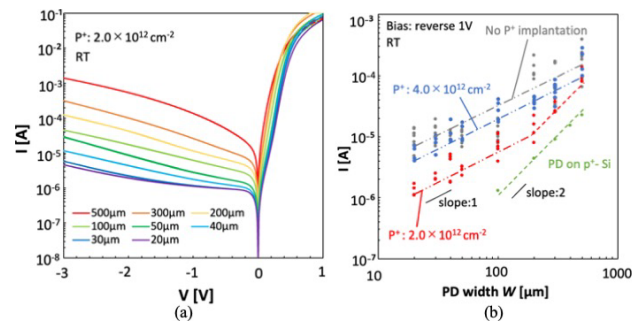


Fig. 6 (a) Typical I-V characteristics of the Ge PDs on n^+ -Si (the P^+ implantation dose of $2.0 \times 10^{12} \text{ cm}^{-2}$) with different PD widths, and (b) the leakage current at the reverse voltage of 1 V as a function of the PD width.

Table 1 A comparison of leakage current of the PDs at 1-V reverse bias.

Sample		$J_{\text{periphery}}$ [mA/cm]	J_{area} [mA/cm ²]
PD on p^+ -Si		N.A.	9.3
PD on n^+ -Si	No P^+ implantation	3.4	N.A.
	P^+ : $2.0 \times 10^{12} \text{ cm}^{-2}$	0.6	30.0
	P^+ : $4.0 \times 10^{12} \text{ cm}^{-2}$	2.0	N.A.

In contrast, the PDs on n^+ -Si without the P^+ implantation as well as those with the P^+ implantation dose of $4.0 \times 10^{12} \text{ cm}^{-2}$ showed the slope of approximately 1, indicating a high peripheral leakage. However, the P^+ implantation with the dose of $2.0 \times 10^{12} \text{ cm}^{-2}$ showed the slope of 2 for the width as large as 200 μm or larger, despite the slope of 1 for the smaller ones. This is a clear evidence of the reduction in the peripheral leakage by the appropriate P^+ implantation. As summarized in Table 1, $J_{\text{periphery}}$ was significantly reduced from 3.4 mA/cm (without the P^+ implantation) to 0.6 mA/cm by implanting P^+ with the dose of $2.0 \times 10^{12} \text{ cm}^{-2}$. However, no significant reduction in the leakage current was observed for the higher dose of $4.0 \times 10^{12} \text{ cm}^{-2}$. This is ascribed to the formation of electron channels because of an overdose to compensate the holes. The implantation dose and/or depth should be optimized for further reducing the leakage current.

To examine the effect of the global P^+ implantation on the photodetection efficiency, I-V curves were obtained under an NIR light illumination, as shown in Fig. 7. Independent of the P^+ implantation, the light illumination at the wavelength of 1550 nm increased the reverse current due to the photocurrent, although at higher reverse voltage ($V <$

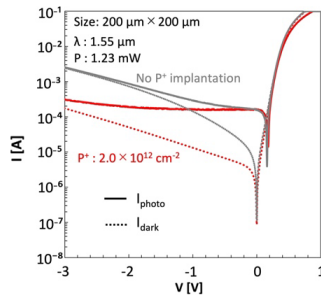


Fig. 7 Typical I-V characteristics of the 200- μm -wide Ge PDs on n^+ -Si with and without an NIR light illumination (1.23 mW at 1550 nm).

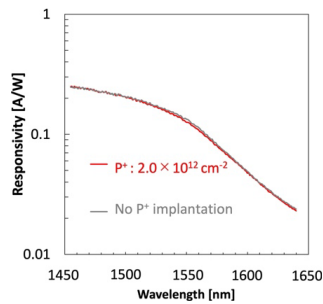


Fig. 8 Typical responsivity spectra at the reverse voltage of 1 V.

–2 V), the current increase was smeared for the PD without the P^+ implantation due to a rapid increase in the leakage current. The responsivity at 1550 nm was estimated to be 0.13 A/W, which is reasonable for the Ge absorption layer as thin as 500 nm. Furthermore, the responsivity spectra at 1455–1640 nm in Fig. 8 were identical between the PDs with and without the P^+ implantation. Therefore, no degradation in the spectral responsivity occurs by the global P^+ implantation, while reducing the dark leakage current in the Ge PDs on n^+ -Si.

5. Conclusion

A reduced dark leakage current, without degrading the NIR responsivity, was realized for a vertical pin structure of the Ge PDs on n^+ -Si substrate. In particular, the peripheral/surface leakage was significantly suppressed by globally implanting P^+ in the i-Si cap layer protecting the fragile surface of i-Ge epitaxial layer before locally implanting B^+/BF_2^+ for the top p^+ region. The P^+ implantation compensates holes at the top Ge surface, preventing the hole conduction from the periphery to the top p^+ region under a negative/reverse bias.

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