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A 20-GHz Differential Push-Push VCO for 60-GHz Frequency Synthesizer toward 256 QAM Wireless Transmission in 65-nm CMOS

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SUMMARY This paper present a 20-GHz differential push-push voltage controlled oscillator (VCO) for 60-GHz frequency synthesizer. The 20-GHz VCO consists of a 10-GHz in-phase injection-coupled QVCO (IPIC-QVCO) with tail-filter and a differential output push-push doubler for 20-GHz output. The VCO fabricated in 65-nm CMOS technology, it achieves tuning range of 3 GHz from 17.5 GHz to 20.4 GHz with a phase noise of −113.8 dBc/Hz at 1 MHz offset. The core oscillator consumes up to 71 mW power and a FoM of −180.2 dBc/Hz is achieved.

key words: *CMOS, push-push VCO, injection locking oscillator, low phase noise, 256 QAM transceiver*

1. Introduction

The demand for high speed wireless communication shows explosive growth due to the increasing using of wireless device for HD video and multimedia transmission. Higher bandwidth and more complex modulation schemes are introduced to satisfy such high speed demand. One promising solution is to utilize 57–66 GHz available band. Recently, increasing higher data rate wireless communication using a 60-GHz CMOS direct conversion transceiver for IEEE 802.15.3c, IEEE 802.11ad/ay have been reported [1]–[4]. In the above transceivers, a 60-GHz local oscillator with quadrature output is necessary, moreover a phase noise of at least −96 dBc/Hz at 1MHz offset is required for local oscillator in order to utilizing 64 QAM modulation scheme [3]. To further satisfy higher speed demand and improve data rate, the wireless system should satisfy the phase noise and SNR requirement for more complex modulation scheme such as 256-QAM to realize 56.32 Gbps at 60 GHz.

In IEEE 802.11ad standard, the requirement of transmitter error vector magnitude (TX EVM) is below −26 dB to support 64 QAM. EVM requirement is proportional to QAM modulation order M when M is high. TX EVM is estimated to be below −32 dB to support 256 QAM. TX EVM can be shown as the equation below [5]:

$$\mathrm{TX\,EVM} = \sqrt{\frac{1}{SNR^2} + \varphi^2_{\mathrm{RMS,eff}}} \tag{1}$$

where SNR is TX signal-to-noise ratio, and $\varphi^2_{\mathrm{RMS,eff}}$ is integrated phase noise of local oscillator. TX SNR usually depends on the backoff of output power, and the phase noise sometimes has a dominant influence on TX EVM. For demodulation, a decision-directed PLL can be used for symbol-timing recovery to cancel low-offset phase noise, and finally relax phase noise requirement. With an optimum tracking bandwidth f_{TRACK} of carrier recovery loop, the effective integrated phase noise can be shown as below [5], [6]:

$$\varphi^2_{\mathrm{RMS,eff}} = 2\int_0^{B/2} \mathcal{L}(f)\left(1 - \frac{1}{1+\left(\frac{f}{f_{\mathrm{TRACK}}}\right)^4}\right)df \tag{2}$$

$\mathcal{L}(f)$ is the phase noise of the carrier. For IEEE 802.11ad, the optimum tracking bandwidth f_{TRACK} is 458.6 kHz. Keeping 3 dB margin, the effective integrated phase noise is −35 dB and resulting a phase noise requirement of 256 QAM for IEEE 80.211ad/WiGig to be less than −102dBc/Hz at 1 MHz offset.

As shown in Fig. 1 conventionally, the quadrature 60-GHz LO generation can be summarized as following methods. In Fig. 1 (a), Ref. [7] proposed a QPLL with in-phase injection-coupled QVCO (IPIC-QVCO) directly oscillat-

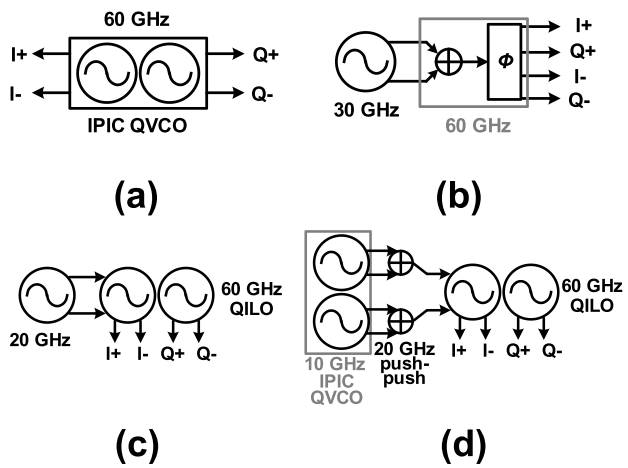

Fig. 1 Conventional 60 GHz quadrature LO generation approaches. (a) 60 GHz IPIC-QVCO (b) 30 GHz VCO + push-push + polyphase filter (c) 20 GHz VCO + 60 GHz QILO (d) 60-GHz QILO using proposed 10-GHz IPIC-QVCO based 20-GHz push-push VCO

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ing at its fundamental frequency of 60 GHz, unfortunately, degradation of LC tank quality factor at millimeter-wave frequency degrades out-of-band phase noise, makes it hard to reach phase noise requirement of 256 QAM. He reports the best phase noise performance to be −91.5 dBc/Hz at 1MHz offset, which supports up to 16-QAM modulation scheme. As shown in Fig. 1 (b), an alternative solution [8] is by employing 30 GHz differential VCO in push-push to generate 60 GHz signal and followed by a polyphase filter to generate quadrature output. However, due to polyphase filter, the resulting large I/Q mismatch makes it inapplicable for complex modulation scheme such as 16-QAM. Figure 1 (c) shows sub-harmonic injection based quadrature injection locked oscillator (QILO). QILO is preferred and frequently used [1]–[5], [9] because of its better phase noise performance, thus 64 QAM can be supported. The reported state-of-art 60-GHz QILO achieves −96dBc/Hz at 1MHz offset, and its corresponding transceiver using 64-QAM modulation scheme achieves highest speed of 42Gb/s as well. However, as information shows explosive growth, there is still demand and improvement of phase noise to reach requirement of 256 QAM. In order to target 256 QAM and realize a phase noise of −102dBc/Hz at 1 MHz offset, Fig. 1 (d) 60-GHz QILO using proposed 10-GHz IPIC-QVCO based 20-GHz push-push VCO can be employed. Due to optimum tank quality factor at 10-GHz, this architecture can improve phase noise performance compared with Fig. 1 (c) 60-GHz QILO using 20-GHz VCO.

In this paper, a 17.5-to-20.5 GHz, −113.8 dBc/H@ 1MHz 20-GHz push-push VCO with 10-GHz IPIC-QVCO with tail filter is proposed and implemented. As shown in Fig. 2, by using proposed 20-GHz VCO in a 20-GHz PLL as sub-harmonic injection to 60-GHz QILO [13], the estimated phase noise at 60 GHz is −104 dBc/Hz at 1MHz offset.

This paper organizes as followed. In Sect. 2, analyses include proposed frequency synthesizer for best phase noise achievement at 60 GHz, 10-GHz IPIC-QVCO with tail filters, 20-GHz differential push-push VCO are introduced. Section 3 explains VCO measurement results. Finally conclusion is drawn for this work.

2. Analysis and Design of VCO

2.1 Design Consideration for Low-Phase-Noise 60-GHz Frequency Synthesizer

Figure 2 shows 60-GHz frequency synthesizer architecture using proposed 20-GHz VCO. There are 2 benefits by employing this architecture. First, the PLL divider N chain can be designed low-frequency and low-power. Second the phase noise will be improved because sub-harmonic 10-GHz QVCO provides phase noise improvement than 20-GHz VCO. Conventionally, 60-GHz quadrature LO in [1]–[5], [9] use a cross-coupled 20-GHz VCO, and the phase noise achieved at 20-GHz is −106 dBc/Hz@1MHz, resulting a phase noise at 60 GHz is −96 dBc/Hz@1MHz. According to Ref. [10], the switched capacitor can be optimized by keeping the same frequency turning range and the same capacitor to transistor size ratio. The inductor quality factor can be adjusted peaking at higher frequency by employing smaller inductor. As shown in Fig. 3, the oscillator overall tank quality factor has an optimum value with different inductor sizes and fixed switched capacitor. The frequency range from 3 GHz to 15 GHz is found to have the best overall tank quality factor. Thus the conventional sub-harmonic injection locked oscillator at 60 GHz can be improved by running fundamental oscillation frequency at range of 3–15 GHz. Considering 60 GHz sub-harmonic frequencies, such as 30 GHz, 20 GHz, 15 GHz, 12 GHz and 10 GHz. For 30 GHz and 20 GHz VCO, the intrinsic tank Q-factor is too low to obtain high phase noise. For 15 GHz, 12 GHz and 10 GHz, VCO needs very high output power to inject into 60 GHz oscillator, the injection locking range will be narrow. In order to obtain both high tank Q-factor and wide locking range, a push-push 20-GHz VCO using 10-GHz QVCO with optimum tank quality factor is proposed. With optimum tank quality factor, a better phase noise performance can be realized using VCO running at 10 GHz instead of at 20 GHz.

Previous work in [13] proposed a tunable second harmonic resonator based 20-GHz VCO shown in Fig. 4. Even

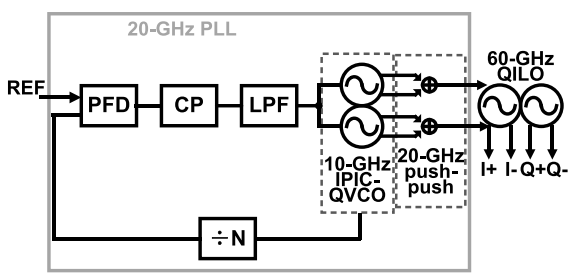


Fig. 2 60-GHz QILO using proposed 20-GHz push-push VCO in a 20-GHz PLL.

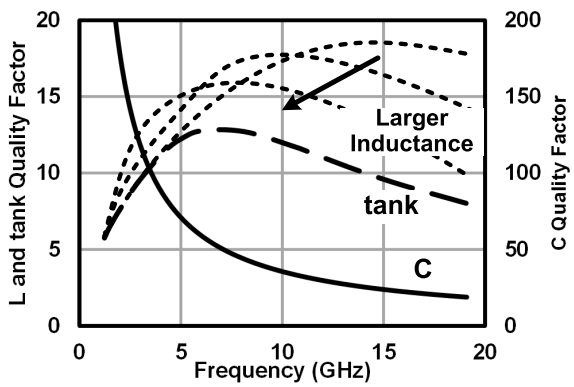


Fig. 3 Quality factor of inductor, capacitor and overall tank for 65-nm CMOS technology presented in [10].

though work in [13] has its fundamental frequency running at 10 GHz sub-harmonic frequency, and extract second harmonic frequency 20 GHz using second harmonic resonator, the phase noise results shown not been improved by the proposed architecture. The main reason is the architecture in [13] using the second harmonic extraction stage for both purpose of harmonic extraction and coupling network. First, as shown in Fig. 4, there will be voltage limit for second harmonic output because core fundamental oscillator and tail cross-coupling shares VDD, headroom for output swing is limited to only 0.5V. The output voltage limit leads to limit of phase noise improvement, because the higher output swing the better phase noise performance can be achieved. Second, the coupling network is running by forcing tail current instead of phase coupling, 10-GHz VCO outputs are not coupled and bias current shown in Fig. 4 has mismatch will leads to high phase error. Third, the coupling network is very weak because the tail transistor has contrary voltages on gate and drain, which will limit the transistor coupling current.

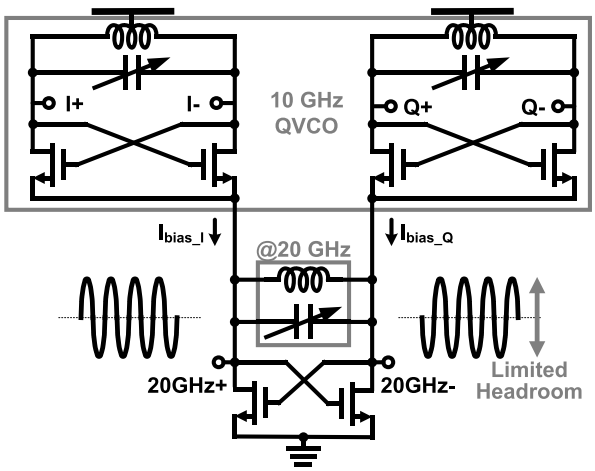


Fig. 4 20-GHz push-push VCO using tunable second-harmonic peaking resonator [13]

This paper proposes 10-GHz in-phase injection-coupled QVCO (IPIC-QVCO) based 20-GHz push-push VCO. Comparing with work [13], fully differential push-push 20 GHz signal is obtained by QVCO followed with push-push stage without sharing current, thus no headroom voltage limit problem and leads to improvement for both output power and phase noise. 10-GHz QVCO and 20-GHz push-push VCO will be discussed in Sects. 2.2 and 2.3 respectively.

2.2 10 GHz IPIC-QVCO with Tail Filters

Figure 5 illustrates the architecture of 10-GHz IPIC-QVCO

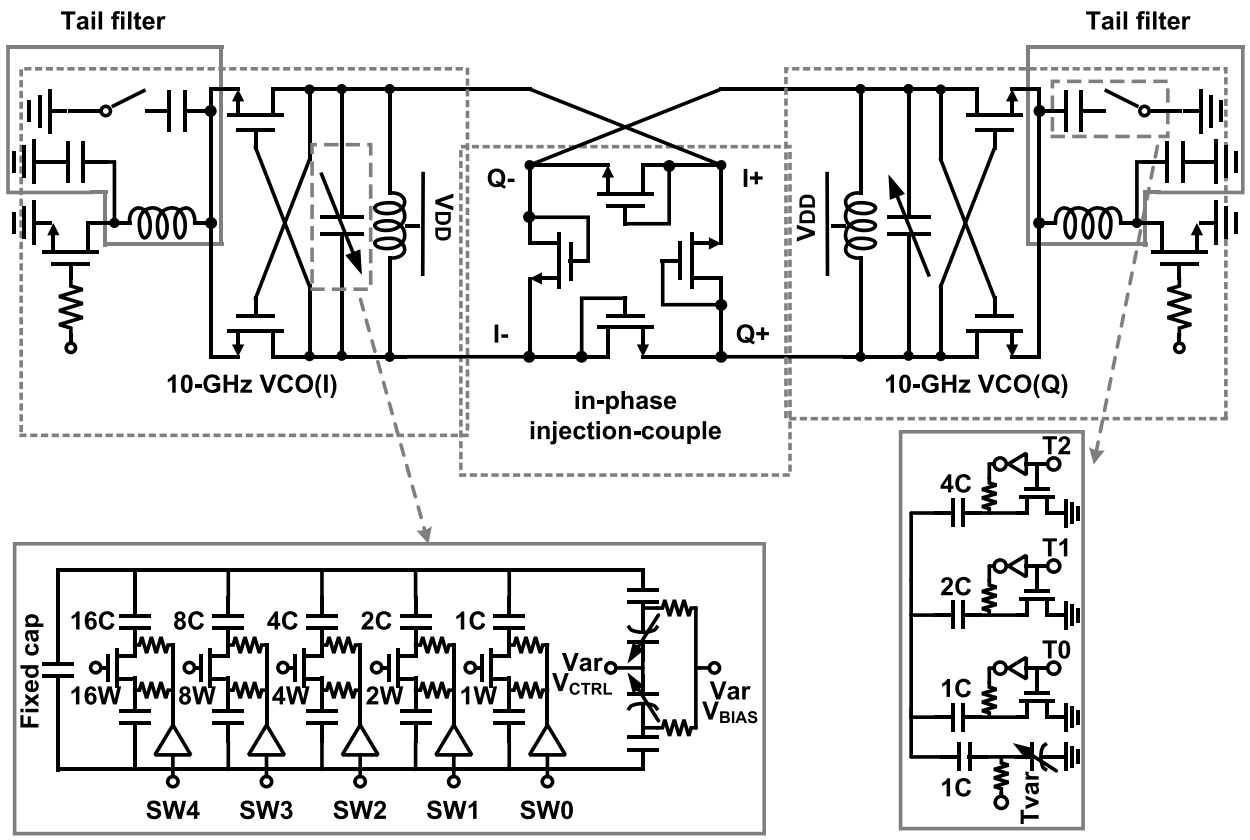


Fig. 5 Schematic of 10-GHz IPIC-QVCO with tail filter and capacitor banks in detail for LC tank and tail filter.

with tail filter. It consists of two 10-GHz cross-coupled LC-VCOs, which are popular due to their relative good phase noise, ease of implementation and differential operation. According to optimization in [10], the inductor in LC resonator tank is chosen to be 200 pH and have an optimum tank quality factor of 25 peaking at 10 GHz. Capacitor and varactor are shown in detail in Fig. 5, fixed capacitor and a 5-bit switching capacitor bank are employed for coarse frequency selection and a varactor employed for fine frequency tuning. Switching capacitor bank is set to 5-bit which allows varactor to be small enough to relax AM-PM phase noise degradation. However, smaller inductance makes smaller oscillation amplitude, in order to improve phase noise performance, the differential pair transistor and tail current source transistor are chosen relative big size. The resulting VCO is finally oscillating in supply limit region. Filtering technique originally proposed in [11] effectively reduce current source noise at 2nd harmonic and relax the loading effect on differential pair in triode region. This design employs tail filter shown in Fig. 5, the tail filter consists of one series inductor and two shunt capacitors. Shunt capacitor beside current source provide path to ground for noise from tail transistor around 2nd harmonic. 3-bit switching capacitor bank and series inductor make impedance at 2nd harmonic to be high enough to prevent tail modulation.

In general, the in-phase coupling quadrature VCO can reduce both white and flicker (1/f) noise by an approximately $\pi/2$ coupling phase shift [12]. In-phase injection-coupling QVCO (IPIC-QVCO) proposed in [7] shows following advantages: low phase noise and phase error; free of RC or LC coupling frequency dependent limitation because $\pi/2$ phase shift network is implemented by transistor instead of RC or LC phase shifter; and lower noise contribution because IPIC-QVCO does not modulate tail transistors in conventional QVCO. However, due to the intrinsic low quality factor characteristic of resonator tank at millimeter-wave frequency, in [7] the proposed IPIC-QVCO oscillating at 60 GHz has limited performance in phase noise improvement. Thus in this proposed 20-GHz push-push VCO design, IPIC-QVCO is employed at 10-GHz with optimum tank quality factor as discussed above. As shown in Fig. 5 10-GHz VCO differential output is connected crosswise with $\pi/2$ phase difference.

The in-phase (I) part and quadrature (Q) part are totally the same with their components and layouts. As given previously, in order to obtain high voltage swing and run 10 GHz fundamental oscillator in supply limit region, the tail transistor M1 for both in-phase and quadrature are chosen with a size of 6um × 32 × 2. According to [7] IPIC coupling network and negative resistance cross-coupled pair are chosen to make a coupling factor 0.27 with corresponding transistor size of 1um × 14 and 2.6um × 20. With 0.27 coupling factor, the IPIC QVCO has have lower phase noise with maintaining small phase error. Note that IPIC QVCO coupling network are self-biased, the schematic and layout can be compact and fully symmetric.

From simulation, as shown in Fig. 6, the average phase noise of entire range of 10 GHz fundamental output in the case of using IPIC coupling network is approximately 2.5dB lower than standalone I part or Q part in QVCO. In other words, QVCO consumes double of standalone VCO power and lower phase noise of standalone VCO by 3dB. Tail-filtering results are simulated and shown as Fig. 6, the benefits of tail-filter is around 1 dB in the entire fundamental frequency range.

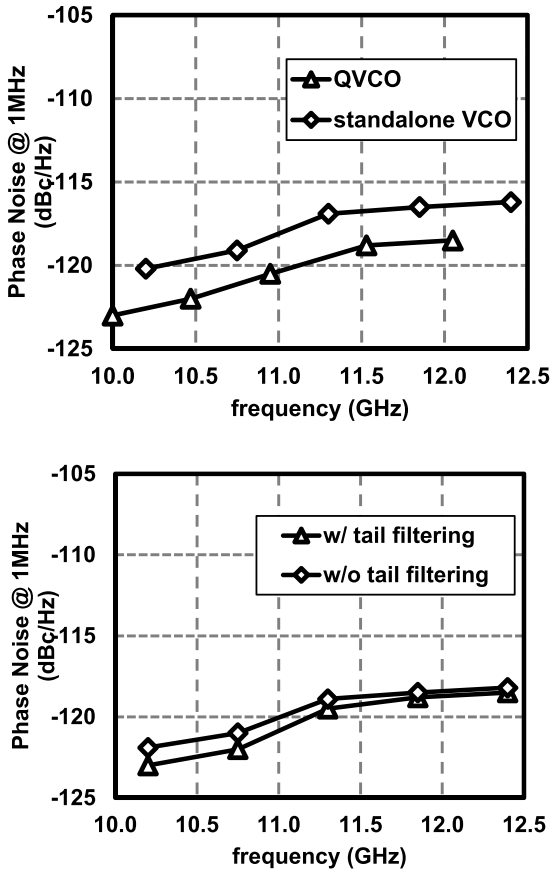


Fig. 6 Simulated phase noise improvement by using quadrature architecture and tail filtering

2.3 Proposed 20-GHz Differential Push-Push VCO Using 10-GHz IPIC-QVCO

This paper employs push-push VCO for 20-GHz frequency generation. The push-push design consists of two fundamental frequency oscillator running at half of the desired output frequency. By using push-push, higher available gain and higher passive component quality factor at lower frequency can be exploited. Such push-push VCOs typically have wider tuning range and lower phase noise. Conventionally push-push VCOs suffer from single-ended output and making it sensitive to noise and other interferences, especially in deep sub-micron CMOS technology, Fig. 7 (a). As discussed before, author in [13] proposed a super-harmonic QVCO based 20-GHz differential push-push VCO, cross-coupled tail transistor are employed to force two fundamen-

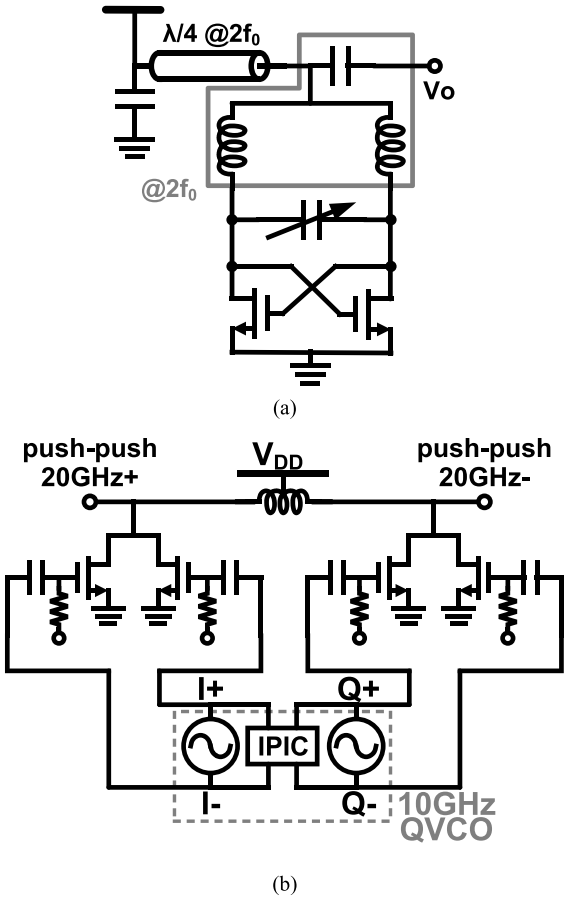


Fig. 7 (a) conventional push-push VCO (b) differential push-push VCO using 10-GHz IPIC-QVCO

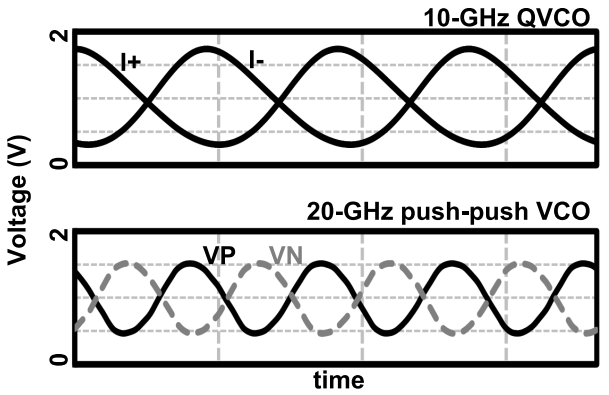


Fig. 8 Simulated 20 GHz push-push output waveform

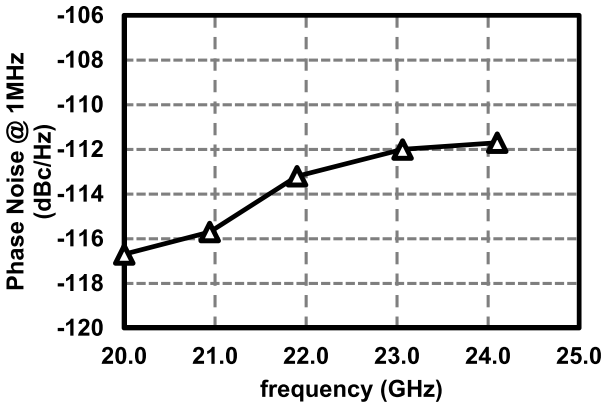


Fig. 9 Simulated 20 GHz push-push VCO phase noise

tal VCO running in quadrature operation. However in this VCO additional LC resonator are needed for second harmonic extraction and frequency tuning. Another drawback is the second harmonic extraction stage has voltage limit which leads to limit improvement of phase noise.

This paper realizes a 20-GHz differential push-push VCO using 10-GHz IPIC-QVCO. As shown in Fig. 7 (b), the in-phase (I) part and quadrature (Q) part of 10-GHz QVCO are connected to two different push-push inputs and generate positive and negative 20 GHz output respectively. Center tap inductor separates 20 GHz differential output and provides VDD supply. The push-push VCO is class-C biased to achieve lower power consumption and higher harmonic output power. Figure 8 shows simulated 20-GHz push-push VCO output waveform corresponding with 10-GHz QVCO output waveform. $\pi/2$ phase difference between two in-phase and quadrature 10 GHz VCOs become π in 2nd harmonic, which is 20 GHz, and the output is fully differential. Figure 9 shows simulated phase noise at 20 GHz output, according to harmonic injection lock theory, phase noise at 20 GHz is accurately 6dB higher than phase noise at 10 GHz. By employing proposed differential 20-GHz VCO as sub-harmonic injection signal in 60-GHz QILO described before, phase noise performance can be further lower instead of using VCO originally running at 20 GHz.

3. Experimental Results

The proposed 20-GHz VCO is fabricated in a standard 65-nm CMOS technology. Figure 10 shows photograph of the fabricated VCO, the total chip area is 720 um × 670 um, and an additional 20 GHz buffer is added to prevent different load impedance from pulling oscillation frequency. The phase noise is measured by using a signal source analyzer (Agilent E5052B) and a dedicated microwave down-converter (Agilent E5053A) for the E5052B.

The proposed 20-GHz VCO covers a frequency range of 17.50 GHz to 20.4 GHz by using a 5-bit switching capacitor bank. Compared with the target frequency band of 19.44 GHz to 21.60 GHz, Measured output frequency is lower than simulation because of underestimated layout parasitic capacitance and inductance in VCO capacitor bank core as shown in Fig. 10, these additional LC will decrease oscillation frequency. Therefore, the 20-GHz VCO used for 60 GHz sub-harmonic injection can cover three 60 GHz band center frequencies (58.32 GHz, 59.40 GHz, and 60.48 GHz).

The measured output power and phase noise is shown in Fig. 11. From 1V supply this VCO observed an average output power of −18 dBm over its frequency

Table 1 Performance comparison

	Architecture	Tech.	Freq. [GHz]	Phase Noise [dBc/Hz] @1MHz	Normalized to 60GHz Phase Noise [dBc/Hz]@1MHz	VCO Power [mW]	VCO FoM [dBc/Hz]	60GHz QAM Supported
[7]	60 GHz PLL using IPIC-QVCO	65nm CMOS	57.9-68.3	-91.5	-	-	-	16 QAM
[3]	60 GHz QILO + 20 GHz PLL	65nm CMOS	58.1-65	-96.5	-	-	-	64 QAM
[6]	60 GHz QILO + 20 GHz SS-PLL	65nm CMOS	55.6-65.2	-93 [a]	-	-	-	64 QAM
[13]	20 GHz push-push VCO	65nm CMOS	16.1-19.6	-106	-96.0 [b]	10.3	-181.3	64 QAM
[14]	20 GHz Class-C VCO	65nm CMOS	19.3-22.4	-105.8	-96.0 [b]	8.7	-182.4	64 QAM
[15]	Current-Redistribution VCO	130nm SiGe	28-37.8	-103.6	-98.4 [b]	10	-193.5	64 QAM
[16]	Inductor Splitting VCO	32nm CMOS	33.6-46.2	-98	-94.5 [b]	9.8	-180	64 QAM
This Work	10 GHz IPIC-QVCO + 20 GHz push-push	65nm CMOS	17.5-20.5	**-113.8**	**-104.2** [b]	71	-180.2	**256** QAM

[a] Estimated from graph

[b] Estimated by normalizing to 60-GHz using sub-harmonic injection lock

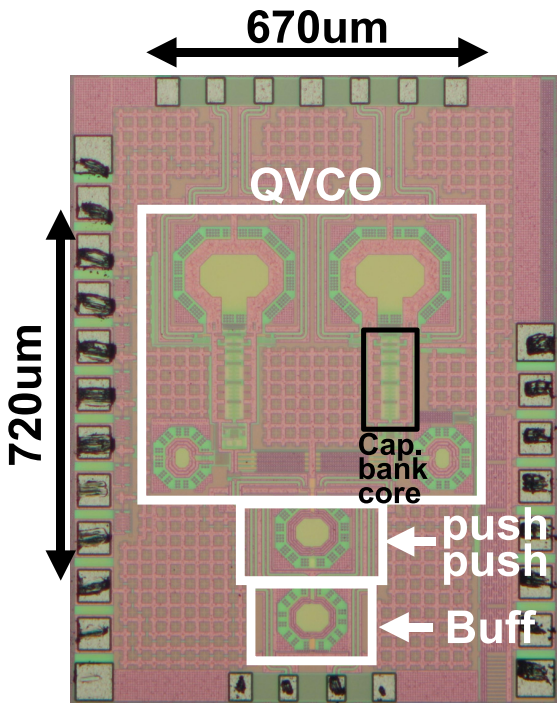
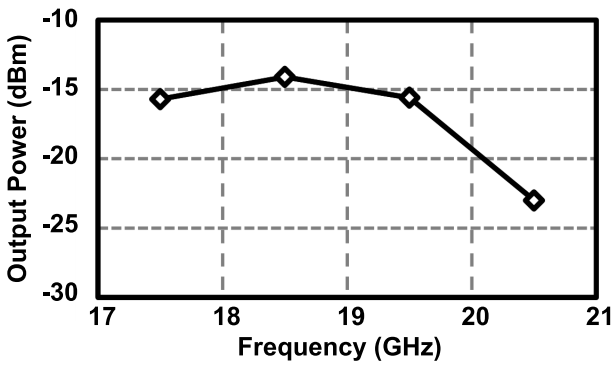
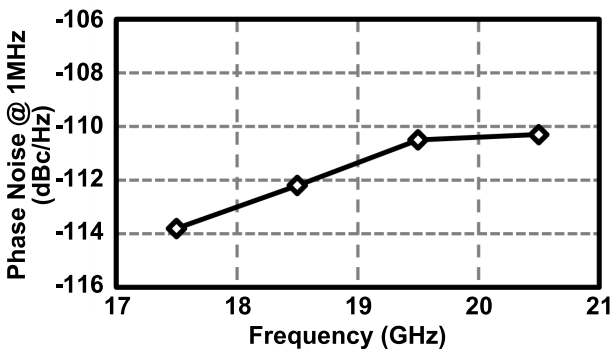


Fig. 10 Photograph of fabricated 20-GHz push-push VCO



(a)



(b)

Fig. 11 Measured 20-GHz VCO (a) output power and (b) phase noise

range, the phase noise achieved is −113.8 dBc/Hz@ 1MHz at 17.5 GHz with 71 mW power consumption, and −110.3 dBc/Hz@1MHz at 20.4 GHz with 61 mW power consumption including 20mW output buffer and 4mW push-push doubler. VCO power consumption increased at lower oscillation frequency because corresponding VCO tank impedance at the oscillation frequency is decreased. The bias voltage at lower frequency is increased to keep oscillator in voltage limit region.

Figure 12 shows measured phase noise results at 10GHz output and the push-push 20GHz output. 10GHz phase noise shares the same noise contribution with 20GHz phase noise because of the harmonic theory. From the measurement results, it is observed push-push 20GHz phase noise is 4 dB to 5 dB degraded from 10GHz phase noise, this relation is close to simulation results. In order to reach sufficient input power for signal source analyzer, 20-GHz LNA with 5 dB NF 20 dB gain is applied for the measure-

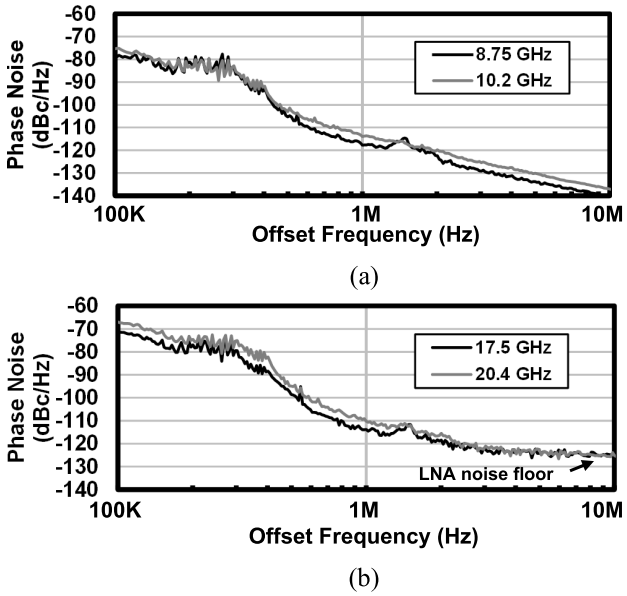


Fig. 12 Measured phase noise results (a) 10GHz (b) push-push 20GHz

ment, and the noise floor is increased.

Overall performances of 60-GHz frequency synthesizers using proposed 20-GHz VCO are compared with other start-of-art 60-GHz LO generations as shown in Table 1. It includes both 60-GHz LO generations and 20-GHz VCOs normalized to 60 GHz using sub-harmonic injection. The normalized phase noise can be calculated by:

$$PN_{\mathrm{QILO}} = PN_{\mathrm{INJ\_OSC}} + 20\log_{10}(N) \quad (3)$$

where N is 3 for 60-GHz QILO with 20 GHz injection. By comparing performance in Table 1, conclusion with previous works and proposed 10-GHz IPIC-QVCO based 20 GHz push-push VCO are summarized as followed: 60-GHz PLL using IPIC-QVCO directly running at 60 GHz which has the least power consumption in reported 60 GHz frequency synthesizer, due to intrinsic low quality factor of overall LC tank, the phase noise performance is not competitive although with IPIC coupling network to improve phase noise. Work [3] and [6] realized 60-GHz QILO using 20-GHz QVCO-PLL as sub-harmonic, and 64-QAM data transmission has also been realized duo to improved phase noise compared with 60-GHz QVCO based PLL. Work [13], [14] also shows as much performance and need further improvement for higher modulation scheme such as 256-QAM. This work using 10 GHz IPIC-QVCO and 20 GHz push-push harmonic output realizes lowest phase noise among 20-GHz VCOs and by using this work for sub-harmonic injection in 60-GHz QILO, the estimated phase noise also achieved the lowest and 256 QAM can be supported according to previous analysis.

4. Conclusion

This paper presents a 20-GHz differential push-push VCO for low-phase-noise high performance 60-GHz frequency synthesizer. The achieved phase noise by using proposed 20-GHz VCO for 60-GHz sub-harmonic injection can satisfy 256 QAM requirement. Therefore more complex modulation scheme and higher data-rate can be applied and achieved in 60-GHz wireless transmission systems.

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