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Silicon Based Millimeter Wave and THz ICs

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SUMMARY In this paper, the research advances in silicon based millimeter wave and THz ICs in the State Key Laboratory of Millimeter Waves is reviewed, which consists of millimeter wave amplifiers, mixers, oscillators at Q, V and W and D band based on CMOS technology, and several research approaches of THz passive ICs including cavity and filter structures using SIW-like (Substrate Integrated Waveguide-like) guided wave structures based on CMOS and MEMs process. The design and performance of these components and devices are presented.

key words: *millimeter wave, THz, amplifiers, mixers, oscillators, substrate integrated waveguide (SIW), half mode SIW (HMSIW)*

1. Introduction

With the rapid advances of silicon based process in recent years, the characteristic frequency f_T and f_{max} have grown into millimeter wave and even THz band. In the next ten years, it could be predicted that the silicon based CMOS ICs will be practicable in millimeter wave band, and partially applicable in sub-millimeter or terahertz band when f_{max} exceeds 1 THz [1]. The reported silicon based millimeter wave IC ranges from 30 GHz to 650 GHz in recent years [2]–[6]. In this paper, we will review the recent advances in silicon based millimeter wave active ICs and THz passive ICs developed in the State Key Laboratory of Millimeter Waves, Southeast University, Nanjing, China.

2. CMOS Millimeter Wave ICs

This section reviews several millimeter wave circuits based on CMOS technology developed in SKLMMW, including amplifiers, mixers, oscillators at Q, V and W and D band.

2.1 Q/V/W-Band CMOS Amplifiers

In the design of millimeter wave CMOS amplifiers, several kind of amplifiers are designed and tested by using IBM 90 nm CMOS technology, including gain stage amplifiers, power amplifiers, and low noise amplifiers at Q, V and W-band. Common source and cascode structure are employed in the design of these amplifiers.

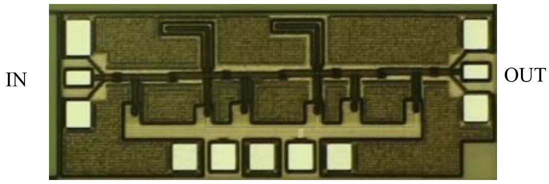

Fig. 1 Photo of three-stage CMOS low noise amplifier (1500 × 550 μm).

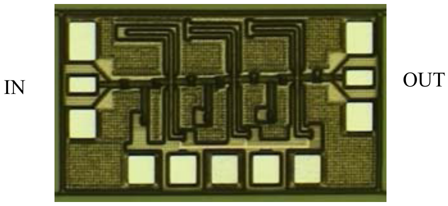

Fig. 2 Photo of three-stage CMOS power amplifier (1050 × 550 μm).

Figure 1 shows a three-stage CMOS low noise amplifier, which employs traditional common-source structure. The measured gain is more than 15 dB in frequency band of 48–60 GHz.

Figure 2 is a three-stage CMOS power amplifier, which is also common-source structure and optimized for power output. The measured gain is more than 15 dB in frequency band of 45–54 GHz, and the output 1dB compression point is more than 8 dBm.

Figure 3 and Fig. 4 show another two CMOS power amplifiers, which employs cascode topology. The first one with two-stage structure, as shown in Fig. 3, has a measured gain of more than 10 dB and output 1 dB compression point of more than 7 dBm at 40–60 GHz. The second one with three-stage structure, as shown in Fig. 4, has a measured gain of more than 20 dB and output 1 dB compression point of more than 9 dBm at 45–56 GHz.

Figure 5 and Fig. 6 show two CMOS gain amplifiers with compact layout using cascode topology. Figure 5 shows a two-stage cascode amplifier, which has a measure gain of more than 15 dB at 45–52 GHz. Figure 6 shows a three-stage cascode amplifier, which has a measure gain of more than 20 dB at 45–60 GHz, and the highest gain exceeds

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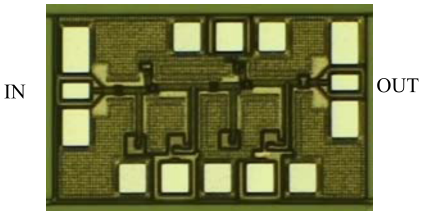


Fig. 3 Photo of two-stage cascode CMOS power amplifier (1000 × 560 μm).

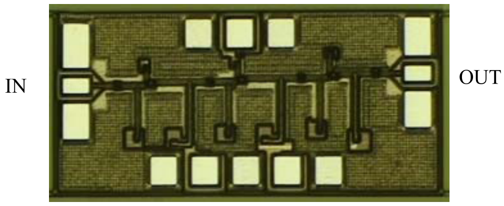


Fig. 4 Photo of three-stage cascode CMOS power amplifier (1280 × 560 μm).

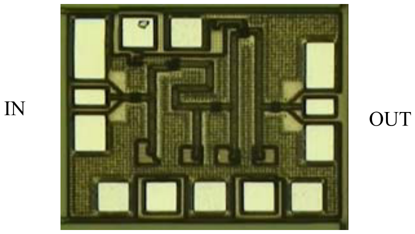


Fig. 5 Photo of two-stage cascode CMOS gain amplifier (780 × 630 μm).

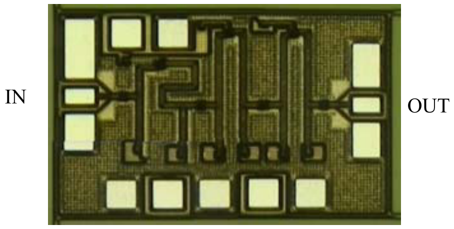


Fig. 6 Photo of three-stage cascode CMOS gain amplifier (970 × 630 μm).

25 dB.

Figure 7–Fig. 9 shows three W-band CMOS gain amplifiers. Figure 7 shows a two-stage cascode amplifier, which has a measure gain of more than 5 dB at 90–107 GHz. Figure 8 is a two-stage common source amplifier, which has a measure gain of more than 5 dB at 90–106 GHz. Figure 9 shows a three-stage common source amplifier, which has a measure gain of more than 10 dB at 95–102 GHz, and the highest gain exceeds 12 dB.

2.2 V/W-Band CMOS Mixers

In the design of millimeter wave CMOS mixers, fundamental and sub-harmonic scheme are employed in circuit topology, four mixers are designed and tested at V-band and W-band by using IBM 90 nm CMOS technology.

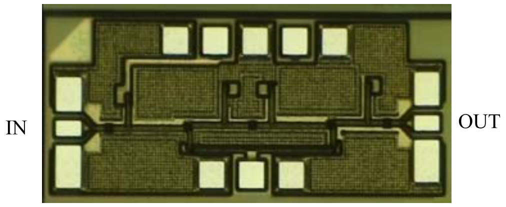


Fig. 7 Photo of W-band two-stage cascode CMOS amplifier (1380 × 570 μm).

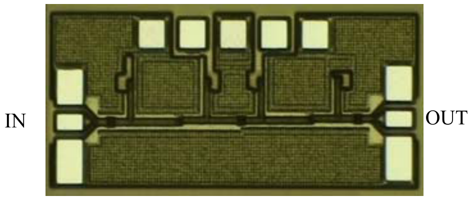


Fig. 8 Photo of W-band two-stage CMOS amplifier (1260 × 550 μm).

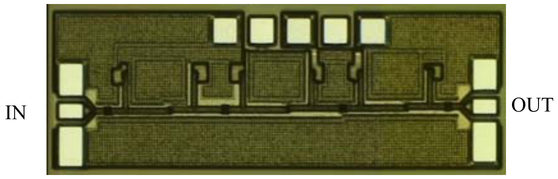


Fig. 9 Photo of W-band three-stage CMOS amplifier (1700 × 550 μm).

Figure 10 and Fig. 11 show two fundamental CMOS mixer at V-band and W-band, using same structure. These mixers employ resistive mixing topology. The LO port is injected at the gate of n-FET and RF is injected at the drain of n-FET, the IF signal is filtered by a LC network at the drain output. The V-band fundamental mixer, as shown in Fig. 10, has a conversion loss of less than 10 dB at 50–75 GHz. The W-band fundamental mixer, as shown in Fig. 11, has a conversion loss of less than 14 dB at 75–110 GHz.

Figure 12 and Fig. 13 show another two CMOS mixer at V-band using sub-harmonic scheme. In Fig. 12, the LO port is injected at the gate of n-FET and RF is injected at the drain, the IF signal is generated by the mixing of LO harmonic and RF signal, and it is filtered by a LC network at the drain output. In Fig. 13, diode pair is used for sub-harmonic mixing, and short/open stubs is used to suppress the unwanted signals. These two mixers has a conversion loss of less than 15 dB at 50–75 GHz.

2.3 V/W/D-Band CMOS Oscillators

In the design of millimeter wave CMOS oscillators, cross-coupled transistors are implemented as the oscillation core, push-push structure is used to get higher output frequency. Two voltage-controlled oscillators (VCO) at V-band and W-band and a fixed frequency oscillator at D-band are designed and tested by using IBM 90 nm CMOS technology.

Figure 14 shows a V-band CMOS VCO using push-

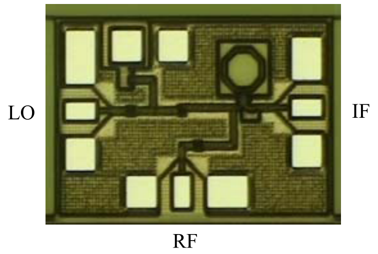


Fig. 10 Photo of V-band fundamental CMOS mixer (800 × 540 μm).

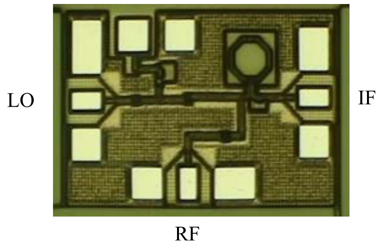


Fig. 11 Photo of W-band fundamental CMOS mixer (800 × 520 μm).

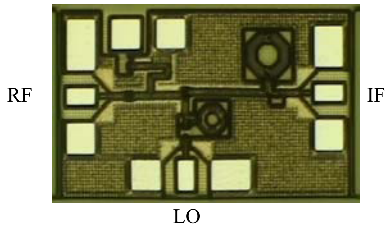


Fig. 12 Photo of V-band sub-harmonic CMOS mixer (890 × 540 μm).

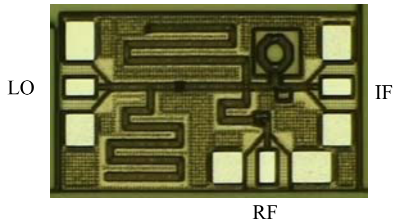


Fig. 13 Photo of V-band sub-harmonic CMOS mixer with diode pair (900 × 500 μm).

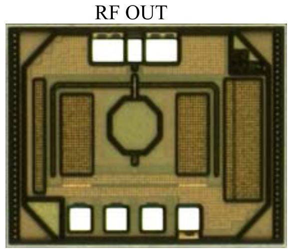


Fig. 14 Photo of V-band CMOS voltage-controlled oscillator (900 × 750 μm).

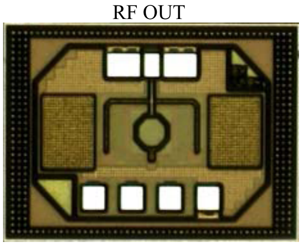


Fig. 15 Photo of W-band CMOS voltage-controlled oscillator (860 × 600 μm).

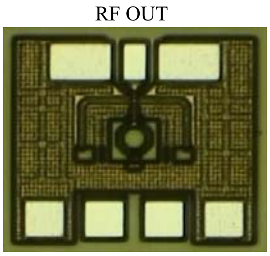
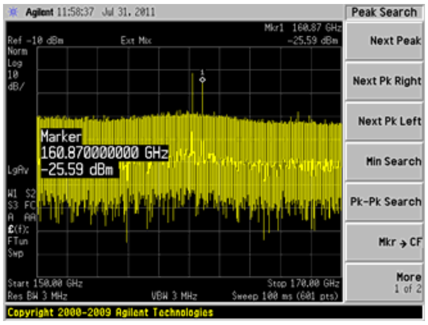


Fig. 16 Photo of D-band CMOS oscillator (560 × 560 μm).



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Mkr1 160.87 GHz

Ref −10 dBm Ext Mix −25.59 dBm

Marker
160.870000000 GHz
−25.59 dBm

Start 150.00 GHz Stop 170.00 GHz

Res BW 3 MHz VBW 3 MHz Sweep 100 ms (601 pts)

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Fig. 17 Measure sprectrum of D-band CMOS oscillator.

push structure, the output frequency is tune by a tunable capacitor at resonance network. This VCO has a measured tuning range of 59–69 GHz, output power of −10 dBm, and phase noise of −103 dBc@10 MHz offset.

Figure 15 shows a W-band CMOS VCO using the similar structure with frequency optimized at W-band. It has a measured tuning range of 93–104 GHz, output power of −20 dBm, and phase noise of −93 dBc@10 MHz offset.

Figure 16 shows a D-band CMOS oscillator using push-push structure and a fixed resonance network due to the lack of tunable devices at D-band. This oscillator is measured with a D-band probe from Picoprobe, and a down-converter form Farran technology. The measure oscillation frequency is around 160.9 GHz, the output power is around −25.6 dBm. Figure 17 shows the measured spectrum.

3. Silicon Based THz ICs

This section reviews several THz circuits around 300 GHz developed in SKLMMW. Base on substrate integrated waveguide technology (SIW), cavities and filters are designed on commercial silicon based CMOS process. Measurement results of fabricated filter shows good performance at 280 GHz on on-chip measurement. Another approach uti-

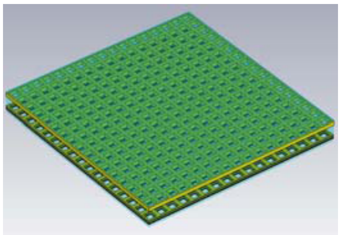

Fig. 18 Cavity model based on IBM 130-nm CMOS technology.

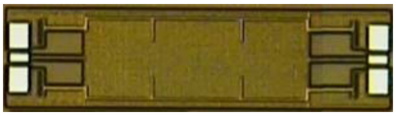

Fig. 19 Photo of a fabricated 280 GHz SIW filter on CMOS (1500 × 400 μm).

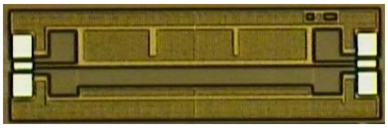

Fig. 20 Photo of a fabricated 280 GHz HMSIW filter on CMOS (1500 × 450 μm).

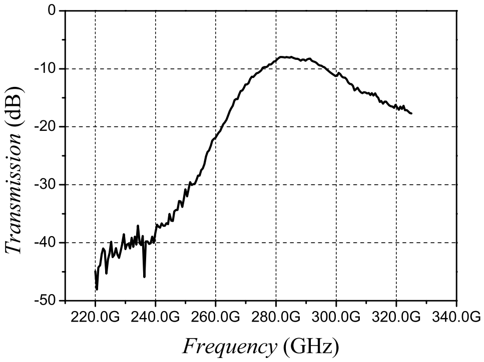

Fig. 21 Measured transmission data of 280 GHz SIW filter on CMOS.

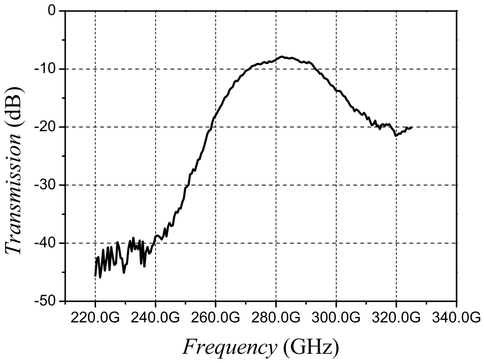

Fig. 22 Measured transmission data of 280 GHz HMSIW filter on CMOS.

lized the merit of high Q cavities using MEMS process and realized antenna and filter on it. Measurement result shows excellent performance at 350 GHz on quasi-optical test.

3.1 Silicon Based THz Filters on CMOS

THz filter is designed by utilizing substrate integrated waveguide technology on CMOS technology. The cavity of SIW is designed using the thick dielectric layers on the process structure, in which the top and bottom plane is utilized by cutting slots in the thick metal layer, in order to fulfill the requirements of the design rule. The cavities and filters are optimized with the process parameters.

A square resonant cavity filled with dielectric was firstly constructed on the chip. But the metallic layer is different from the usual SIW, since the metallic layers on chip cannot have a large size without a slot or a window. The design rules also require that the ratio of metal area to dielectric area fall in a given range. So the cavity has been designed with metallic layer modified, as shown in Fig. 18. The side wall is constructed by rows of via, which is similar to usual SIW cavities. The upper and lower metallic layer of cavity is a period contracture. The dielectric layer utilized the silicon oxide and nitride layer between MA and LY layer of IBM 130 nm CMOS process. In this cavity, the dominant mode TE101 could be simulated by eigen-mode method. The resonant frequency is found to be lower about 3% than usual cavity at 300 GHz. And the estimated Q value is about 60.

According the estimation, the cavity is suit for design filter with a fractional bandwidth great than 3%. A SIW filter and a half-mode SIW (HMSIW) filter based on CMOS is design and fabricated, as shown in Fig. 19 and Fig. 20. The size of HMSIW is around half the size of its counterpart SIW [7]–[11]. These two filter chips are measured using an on-chip measurement setup provide by the City University of Hong Kong. Only transmission data is retrieved from measurement because of the calibration problem in this setup. From the measured data in Fig. 21 and Fig. 22, the insertion loss of SIW and HMSIW filter is estimated lower than 5 dB if we take account of the SIW-microstrip transition loss and microstrip loss at each port.

3.2 Silicon Based THz Antenna and Filter on MEMS

A silicon based THz SIW bandpass filter is designed by using high Q cavities of MEMS process. In order to couple signals from quasi-optic test, a pair of linearly tapered slot antennas (ALTSA) are designed. The integrated antenna and filter are then fabricated with MEMS process and tested around 360 GHz.

Figure 23 shows the filter model based on CST software. It is a dual mode filter with circular cavities [12], [13]. Simulation shows very low insertion loss of the filter about 0.3 dB around 356 GHz, because of the high Q-factor (estimated 1000).

A pair of antennas must be connected at the input and output ports for a quasi-optic test setup. As shown in Fig. 24, a wideband ALTSA is chosen and a triangle taper is de-

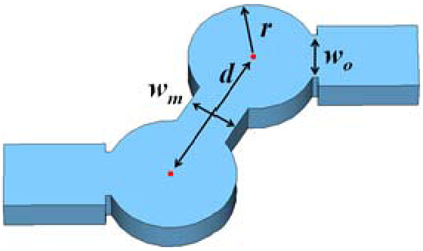

Fig. 23 CST model of the filter with $w_m = 0.400$ mm, $w_o = 0.390$ mm, $d = 1.223$ mm and $r = 0.480$ mm.

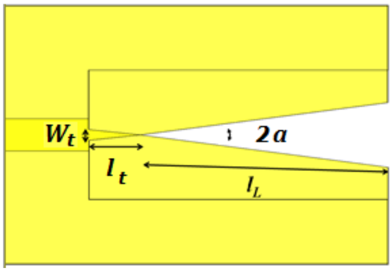

Fig. 24 The configuration of the ALTSA with $w_t = 0.183$ mm, $l_t = 0.917$ mm, $2\alpha = 14°$ and $l_L = 4.400$ mm.

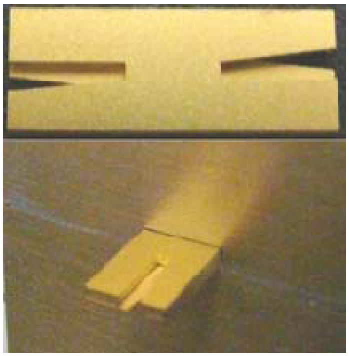

Fig. 25 Photo of the prototype and the fixture for measurement.

signed as the transition between the filter input/output and ALTSA [14], [15].

An integrated prototype with passband range 350 GHz ~ 370 GHz is designed and fabricated with MEMS process, as shown in Fig. 25. It is measured by using a quasi-optic testing system. The measured data is in agreement with the simulated result, which shows the filter has good selection performance and verified the wideband characteristic of the ALTSAs, as shown in Fig. 26.

Acknowledgments

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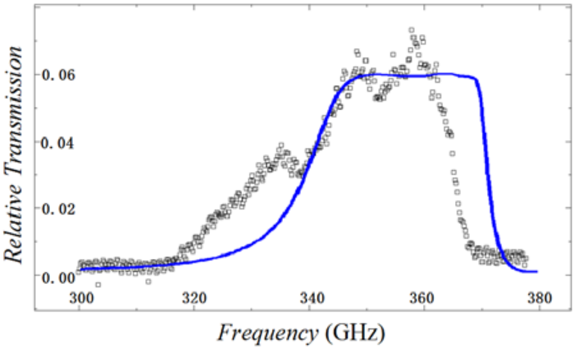

Fig. 26 Measured relative transmission magnitude (dotted line) compared with simulation (solid line).

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