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Independent-Double-Gate FinFET SRAM Technology

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SUMMARY Multi-Gate device technology is the promising candidate for the enhancement of device characteristics of the scaled MOSFETs. Moreover, independent-double-gate devices have been proposed to achieve flexible V_{th} adjustment. It is revealed that the SRAM noise margins have been increased by introducing the independent-double-gate FinFET.

key words: *multi-gate devices, FinFET, SRAM, noise margin*

1. Introduction

Due to the rapid reduction of the feature size of complementary metal oxide semiconductor (CMOS) devices, device technology is facing several difficulties. Short channel effects (SCEs) such as the threshold voltage roll-off and the sub-threshold slope (s-slope) degradation caused by the reduced drivability of the gate electrode cause significant increase in power consumption and become a limiting factor in MOS devices. In addition, variability of the CMOS device is increasing and reduces the yield of the CMOS circuit. Especially, the SRAM cell uses the smallest transistor to achieve high density integration and the yield of the SRAM cell is rapidly decreasing. Thus, reduction of the SCE, standby power consumption, and variability is becoming the most important issues in CMOS devices. In this report, we review the effectiveness of introducing multi-gate device especially independent gate device in the SRAM cell.

2. Advantage of the Multi-Gate Device

To enhance the short-channel effects immunity and reduce the leakage current of the scaled MOSFET, double-gate (DG) device technology has firstly been invented by Sekigawa et al. in 1980 [1]. The channel region of the device is sandwiched by a double-gate. The double-gate structure increases the electrostatic controllability and effectively controls the channel potential and reduces the short channel effects. Figure 1 shows an original concept of the double-gate devices. They named this device as a XMOSFET and they improved the characteristics by using a vertical channel as shown in Fig. 2 [2], which is known as a FinFET. They succeeded in fabricating the double-gate devices and showed the superiority of the device characteristics in 1985 [3].

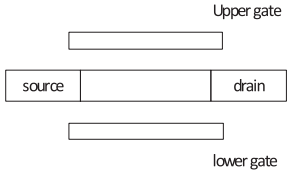

Fig. 1 A schematic illustration of the original invention of the double-gate device.

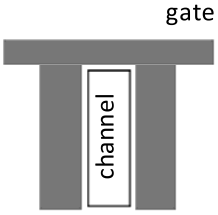

Fig. 2 A schematic illustration of the vertical channel double gate device.

In 1989, Hisamoto et al. reported a fully depleted lean-channel transistor (DELTA) SOI MOSFET using the vertical channel and the double-gate configuration [4]. By using this configuration, the self-aliened double-gate can easily be fabricated. In 1998, he and his coauthors also reported a folded channel MOSFET [5] with the vertical ultra-thin channel and the double-gate. They called the folded vertical channel as a "Fin", and which become common for representing the vertical silicon ultra thin channel. Currently, the FinFET with the double-gate and the upstanding "Fin" becomes common MOSFET thanks to its high process compatibility with the conventional MOSFET.

Superiority of the double-gate device is also predicted by the calculation. Sub-threshold swing degradation and other short channel effects such as the reduction of the V_{th} are caused by the encroachment of electric field lines from the source to the drain. Yan et al. introduced a natural length that controls the spread of the electric filed in the channel direction [6]. The natural length of the single gate MOSFET is described by (1) while that of the double gate device is described by (1).

$$\lambda_1 = \sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{ox}} t_{ox} t_{si}} \tag{1}$$

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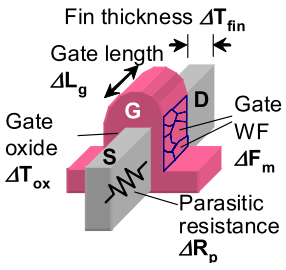

Fig. 3 A schematic illustration of the variation sources in the FinFET.

$$\lambda_2 = \sqrt{\frac{\varepsilon_{Si}}{2\varepsilon_{ox}} t_{ox} t_{si}} \tag{2}$$

It is reported that the effective gate length of a MOSFET device must be larger than 5 to 10 times the natural length to prevent short channel effects and produce a reasonable sub-threshold behavior [6]. According to (1) and (2), the natural length of the double-gate device is much smaller than that of the single gate device and therefore the double gate device effectively suppress the short channel effects. In addition, increasing the number of the gate electrodes further suppresses the short channel effects and the triple gate device or eventual surrounding gate device have also been proposed as one of the multi-gate devices [7], [8].

In addition to the better short channel control, the multi-gate device can reduce the variability in device characteristics. Due to the better electrostatic controllability of the channel potential, the multi-gate device allow the use of the intrinsic channel with no dopant and the non-doped channel effectively suppress the random dopant fluctuation which is the main cause of the variation in the current bulk MOSFETs. The variability issues are summarized in Fig. 3. The variability is caused by the dimension variations such as gate length, channel thickness, and gate oxide thickness [9], [10]. Also, it is caused by the random dopant fluctuation in the channel [11], [12], and work-function variation due to the granularity of the gate-electrode [13]–[16]. The metal gate (MG) electrode has become a primary technology for the advanced CMOS application to suppress gate depletion, control the threshold voltage ($V_{\rm th}$), and overcome incompatibility of the poly-silicon gate to high-k materials. However, using the MG introduces a new variation due to the dependency of the work function (WF) on the orientation of metal grains.

The variability of the MOSFET is characterized by the Pelgrom plot [17]. In this plot, standard deviation of the threshold voltage ($\sigma V_{\rm th}$) is plotted as a function of the square root of the inverse channel area $1/(L_{\rm G} x W_{\rm G})$ where $L_{\rm G}$ is the gate length and $W_{\rm G}$ is the gate width since the $sV_{\rm th}$ is represented by (3).

$$\sigma V_{th}^2 = \frac{Avt}{LW} + B \tag{3}$$

The slope of the Pelgrom plot called Avt represents the variation of the MOSFET in the certain device fabrication technology. Figure 4 shows the benchmark of the Avt. The

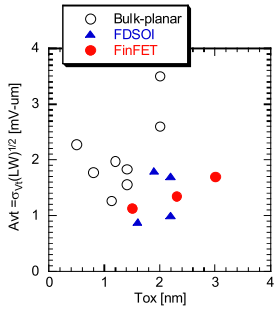

Fig. 4 A benchmark of the Avt value.

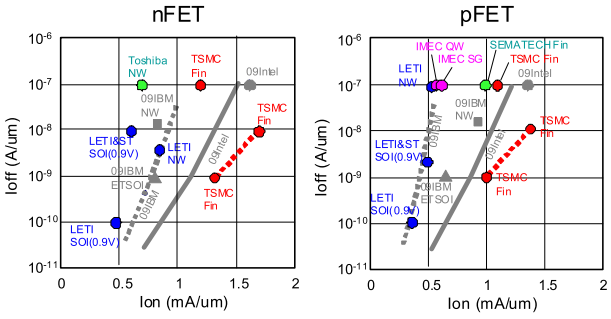

Fig. 5 Ion-Ioff plot of the scaled transistors; (a) nFET, (b) pPET.

multi-gate device such as the FinFET and fully depleted SOI (FDSOI) devices provide smaller Avt due to the intrinsic channel.

If we use the typical (100) Si wafer, the vertical channel orientation is ⟨110⟩. The previous literature indicates that the hole mobility on the (110) surface is higher than that of the (100) surface [18]. On the other hand, the electron mobility on the (110) channel degrades. However, this degradation is not an issue thanks to the recent channel engineering technology. The electron and the hole mobility on the (110) channel can be effectively improved by adding stress by the stressor materials [19]. Figure 5 shows the $I_{\rm on}/I_{\rm off}$ plot of the FinFET. Thanks to the excellent high-k/metal-gate gate stack fabrication technology and the excellent channel engineering to introduce stress, the superior on-current ($I_{\rm on}$) with the reasonable off-current ($I_{\rm off}$) is realized.

3. The FinFET SRAM Cell

3.1 Advantage of the FinFET SRAM Cell

Recently, scaled SRAMs are confronted with a severe degradation in the cell stability which affects the yield of LSIs because the SRAM cells use the smallest transistors and occupy a considerable part of the LSI. Due to these advantages of the double-gate devices, many studies have focused on the FinFET SRAM cells to overcome the rapid decrease in the conventional SRAM performance [19]–[23]. The influence of FinFET variability on the SRAM performance has also been studied [13], [24]. Figure 6 summarizes the reported cell size for the scaled FinFET SRAM. Drastic re-

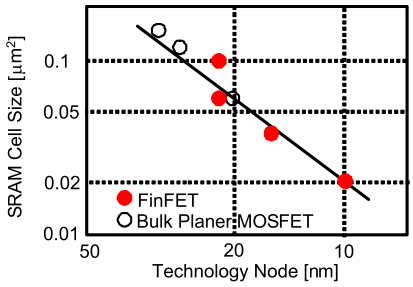

Fig. 6 The reported SRAM cell size as a function of the technology node.

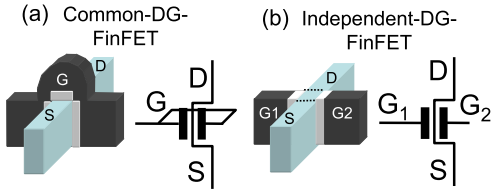

Fig. 7 Schematic illustrations of the FinFET; (a) common DG FinFET, (b) independent DG FinFET.

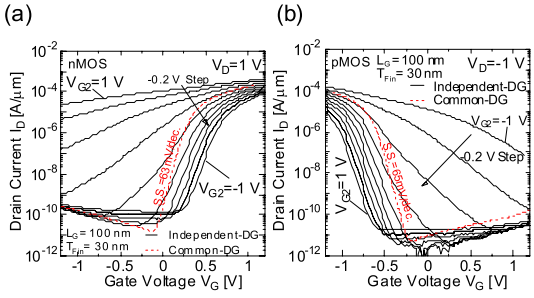

Fig. 8 I_D-V_G characteristics of the FinFETs; (a) nMOS, (b) pMOS.

duction of the SRAM cell size can be realized thanks to the excellent SCE immunity of the FinFET. However, the SRAM operation is not free from the trade-off relationship between the read and the write margins even for the FinFET SRAMs. Thus, a new method to enhance the stability is required. This will be realized by dynamically controlling the threshold voltage (V_{th}) of the pass gate. The following section describes new SRAM cells with the independent-double-gate devices.

3.2 Independent-DG FinFET SRAM Cell

In 2004, Liu proposed a V_{th} controllable four terminal (4T) FinFET with the independent double-gate (DG) by separating the connection between the common DG [25]. One gate electrode can be used as a signaling gate and the other gate can be used as a V_{th} control gate as schematically shown in Fig. 7(b). The chemical mechanical polishing process and the etching based process has been carried out for the gate separation [25], [26]. Figure 8 shows the current-voltage characteristics of the conventional common-DG (CDG) FinFET and the independent-DG (IDG) FinFET with various biasing condition for the V_{th} control gate. Flexible control of

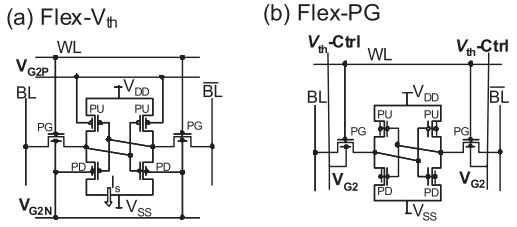

Fig. 9 Schematic illustrations of the SRAM cell.

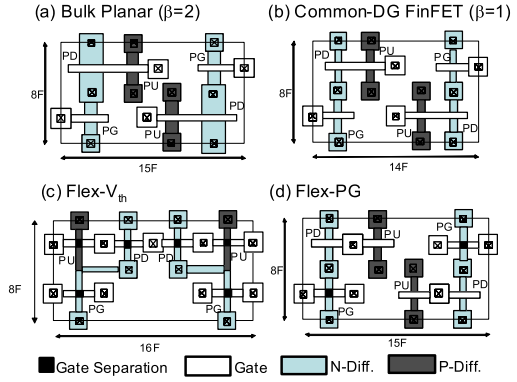

Fig. 10 Proposed layouts for the SRAM cell; (a) bulk planer, (b) CDG-FinFET, (c) Flex-Vth, (d) Flex-PG.

the V_{th} of the FinFET by the control gate can be clearly seen. It should be noted that the values of V_{th} shift rate γ defined by $-\Delta V_{th}/\Delta V_{G2}$ is higher than that obtained by the conventional body-bias control of the planar MOSFETs [27].

Figure 9 shows the schematic topologies of the FinFET SRAM cells using the IDG-FinFET. One is a flexible-V_{th} (Flex-V_{th}) SRAM cell (Fig. 9(a)) [28] and the other is a flexible pass-gate (Flex-PG) SRAM cell (Fig. 9(b)) [29], [30]. In the Flex-V_{th} cell, all the transistors in the cell are composed by the IDG-FinFET. The V_{th} of the all transistor can be controlled by the external bias to the V_{th}-control-gate (V_{G2N} and V_{G2P}). For the Flex-PG cell, IDG-FinFETs are used only for the PG and the other transistors are composed by the common-DG FinFET. The Ion ratio of the pull down to the pass gate which corresponds to the β-ratio is thus flexibly changed. The V_{G2} lines to control V_{th} are implemented parallel with the bit lines and the V_{th} control is executed column-by-column. In the read operation, the corresponding β-ratio is increased by raising the V_{th} of the pass gates. On the other hand, in the write operation, the write margin is enhanced by lowering the V_{th} of the pass gates. Consequently, the V_{th} flexibility in the pass gate makes the SRAM cell free from the trade-off relationship between the read and the write margins. Although additional contact areas are needed for the IDG-FinFET cells, total cell areas are comparable to the bulk cell as shown in Fig. 10. It should be noted that, for the Flex-V_{th} and Flex-PG SRAM, additional V_{th}-control lines are required to supply the bias voltage to the accessed cell.

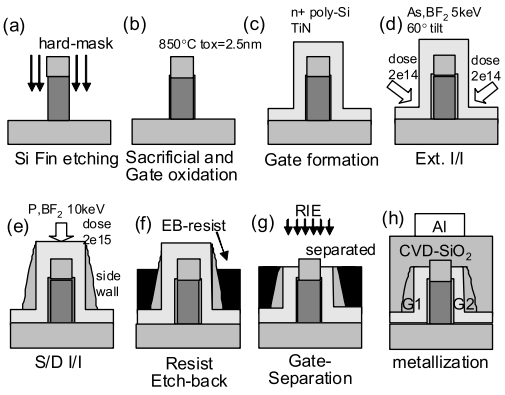

Fig. 11 Schematic device fabrication processes for the FinFET.

3.3 Fabrication of the SRAM Cell

We used lightly dope p-type (100)-oriented silicon-on-insulator (SOI) wafers; thus, the channel-orientations of the fabricated FinFETs were (110). Schematic device fabrication processes are shown in Fig. 11. A 50-nm-thick non-doped silicate glass (NSG) layer and the electron beam (EB) resist masks were formed to make hard masks on the wafer. To fabricate vertical Si-Fins, the SOI layer was etched by a conventional reactive ion etching (RIE) using a Cl_2 inductively coupled plasma (ICP) as shown in Fig. 11(a). After the Si-Fin etching, a 2.5-nm-thick gate-oxide was formed at 850°C followed by the TiN and n+ polycrystalline-Si (poly-Si) gate formation using EB lithography and the RIE. After the gate electrode was formed, a shallow implantation into the extension of the source/drain (S/D) was performed. To distribute impurity atoms (BF_2 for pMOS and As for nMOS) uniformly into the vertical channel, 60-degree tilted implantation was carried out at an acceleration energy of 5 keV and a dose of $2 \times 10^{14}\,\mathrm{cm}^{-2}$ in each side [31]. A 1-nm-thick screening oxide was used to suppress the significant dopant loss [32], [33]. A S/D implantation was performed at an acceleration energy of 10 keV and a dose of $2 \times 10^{15}\,\mathrm{cm}^{-2}$ after a 50-nm-thick gate-sidewall was formed by using CVD grown SiO_2. The acceleration energy was set to 10 keV to preserve the seed-crystal layer for the recrystalline annealing.

Then, the poly-Si gate for the IDG-FinFET was separated by using a newly developed resist etch-back process [26] whereas the CDG-FinFET region was protected by a thicker photo-resist. Due to the three-dimensionally shaped Si-Fin, the thickness of the spin-coated EB resist was thinner at the top of the Si-Fin than that at the other planar portion. Consequently, the poly-Si gate at the top of the Si-Fin was revealed by the partial ashing of the EB resist as shown in Fig. 11(f). After the poly-Si gate was revealed by thinning the EB resist, the poly-Si gate was separated using RIE with HBr based chemistry and the poly-Si gate over the Si-Fin connected to the each side of the gate was completely removed. Finally, the S/D was activated at 830°C for 2 seconds and the devices were sintered at 450°C in 3% H_2 ambient after the metallization. Figure 12 shows the cross sectional transmission electron microscope (TEM) image of the fabricated FinFET and the plane scanning electron microscope (SEM) image of the SRAM cell.

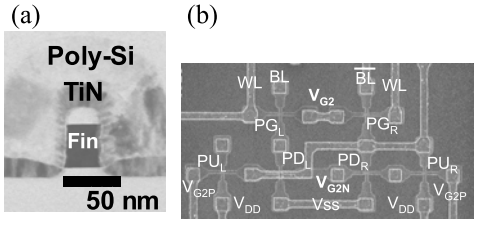

Fig. 12 A cross sectional TEM image of the FinFET (a) and a plane SEM image (b) of the SRAM cell.

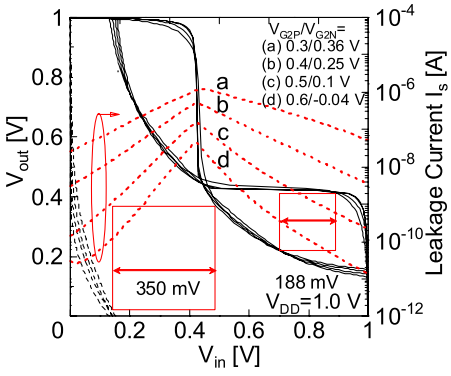

Fig. 13 Experimental butterfly curves and short circuit currents of the Flex-Vth cell as a function of various biasing conditions.

3.4 Characteristics of the SRAM Cell

The concept of the new SRAM cell with the IDG-FinFET is to dynamically reduce the SRAM leakage current using the Flex-V_{th} cell. Figure 13 shows the experimental butterfly curves and short circuit currents with various biasing conditions. By applying opposite bias voltages to the pMOS and nMOS IDG-FinFETs (V_{G2N} and V_{G2P}), the real values of V_{th} can be tuned keeping the symmetry of V_{th}. Thus, the stand-by leakage current and the short circuit current of the cell are dynamically controlled maintaining the same noise margin. The lower stand-by current is appropriate for the stand-by cell, and the high power operation is applicable for the accessed cell to maintain access speed.

The next concept is to dynamically control the PG to enhance noise margins. A great enhancement of the read margin is experimentally confirmed by lowering the V_{G2} as shown in Fig. 14(a). In addition, by increasing the V_{G2} for the PG, the highest write margin can be obtained as shown in Fig. 14(b). To clarify the effects of the V_{G2}, the read and write margins are summarized as a function of the V_{G2} as shown in Fig. 15. During the read operation, applying the V_{G2} of 0 V enhances the read margin, while the V_{G2} of 1 V during the write operation increases the write margin. Thus, enhancement of both the read and write margins by controlling the appropriate V_{G2} is clearly confirmed. These experi-

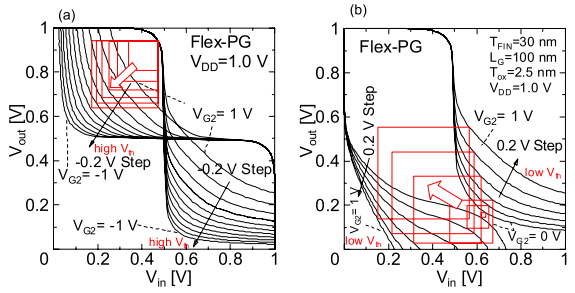

Fig. 14 Experimental butterfly curves for the read margin (a) and write margin (b) evaluation with various V_{G2} conditions.

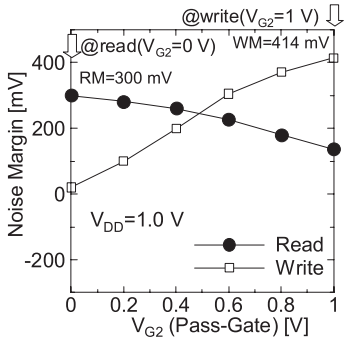

Fig. 15 Experimental noise margins as a function of the VG_2 for the pass gate.

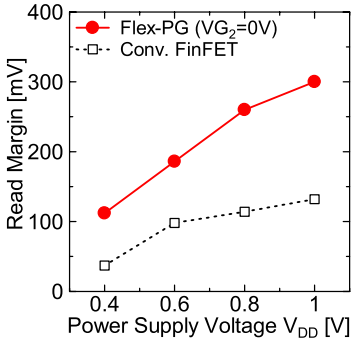

Fig. 16 Comparison of the read margin as a function of the supply voltage.

mental results approve the effectiveness of the Flex-PG cell for suppressing the trade-off relationship of read and write margins. Figure 16 summarizes the V_{DD} dependence of the read margins for the evaluated SRAM cells. The read margins of the IDG-FinFET SRAM cells are much higher than that of the standard FinFET SRAM cell.

4. Variability Issues

4.1 Variability Issues in the FinFET

As mentioned in the introduction, the FinFET uses the non-dope channel and thus the random dopatnt fluctuation can be avoided. However, variability of the FinFET occurs and its origin has not been understood well. Possible variation sources are fluctuations of the gate-length (ΔL_G), the fin-width (ΔT_{Fin}), the oxide thickness (ΔT_{ox}), the line edge roughness of fin and gate electrodes, random dopant, and work-function variation as already shown in Fig. 3. Recently, a mid-gap TiN MG is commonly used to adjust the V_{th} of the CMOS FinFET with an undoped channel. Therefore, it is valuable to comprehensively analyze variability in the TiN MG FinFET. In addition to the V_{th} variation, the on-current variation (ΔI_{on}) will also affect the circuit performance. The ΔI_{on} is caused not only by the ΔV_{th}, but also by the parasitic resistance variation (ΔR_p) and the ΔT_{ox}. In this paper, we thoroughly investigate variability in the TiN MG FinFET.

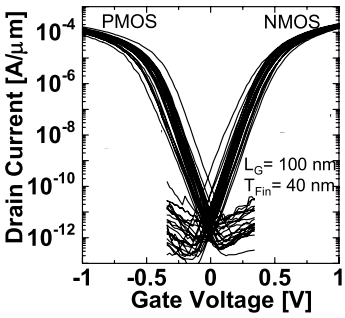

Fig. 17 I_D-V_G characteristics of the TiN Metal-Gate FinFET.

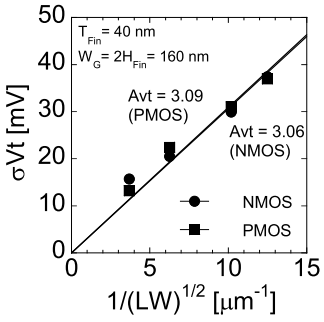

Fig. 18 Pelgrom plot of the FinFET.

Figure 17 shows typical I_D-V_G characteristics of the fabricated FinFETs. Although variation of characteristics exists, symmetrical characteristics of pMOS and nMOS FinFETs are realized thanks to the mid-gap TiN MG. A considerable V_{th} variation is clearly seen even for the undoped channel FinFET. Figure 18 shows the Pelgrom plot. It exhibits a linear relationship indicating that the variation increases with scaling of gate area. It is noteworthy that the slopes of the Pelgrom plot (A_{vt} values) of undoped pMOS and nMOS FinFETs are almost the same as shown in Fig. 18. This is much different from those in the case of the doped-channel in which the channel doping induces a larger V_{th} variation for the nMOS than that of the pMOS transistor due to the transient enhanced diffusion (TED) of boron in the nMOS transistor [34], [35].

To understand the origin of the V_{th} variation in the TiN MG FinFET, we experimentally evaluate the effect of the ΔL_G, ΔT_{Fin}, and ΔT_{ox} to the V_{th} variation by measuring

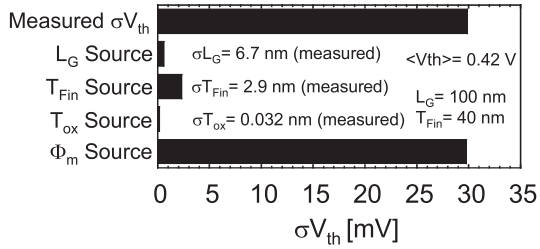

Fig. 19 $V_{\rm th}$ variations due to the $\Delta L_{\rm G}$ $\Delta T_{\rm Fin}$ and $\Delta T_{\rm ox}$. These values are small indicating that the dominant $V_{\rm th}$ variation source is the WFV.

the standard deviation of these values. The effect of these components can be evaluated since the overall $V_{\rm th}$ variation ($\sigma V_{\rm th}$) is divided by its components as indicate by the error propagation law (4).

$$\sigma V_t^2 = \left(\frac{\partial Vt}{\partial L_G}\sigma L_G\right)^2 + \left(\frac{\partial Vt}{\partial T_{Fin}}\sigma T_{Fin}\right)^2 + \left(\frac{\partial Vt}{\partial T_{ox}}\sigma T_{ox}\right)^2 + \left(\frac{\partial Vt}{\partial \Phi_m}\sigma \Phi_m\right)^2 \quad (4)$$

The standard deviations of the dimension variation sources such as the $\Delta L_{\rm G}$ and $\Delta T_{\rm Fin}$ were measured by counting the statistical distribution of the size using a scanning electron microscope (SEM). The same chip is used after the electrical measurements. The $\Delta T_{\rm ox}$ variation was measured by ellipsometry using (110) oriented test wafers which have the same orientation with the side-wall channel of the FinFET. Partial derivatives in (4) were evaluated by measuring the dependence of the $V_{\rm th}$ with the $L_{\rm G}$, $T_{\rm Fin}$, and $T_{\rm ox}$. The experimental results of these contributions are summarized in Fig. 19. It is revealed that the $\Delta L_{\rm G}$, $\Delta T_{\rm Fin}$, and $\Delta T_{\rm ox}$ contributions to the $V_{\rm th}$ variation are insignificant since their standard deviations and partial derivatives are small. Thus, it is concluded that the main variation source of the TiN MG FinFET is the work function variation (WFV) of the TiN. The observed $\sigma\Phi$m of 30 mV is almost the same value with the previous reports [14], [15]. The possible explanation of the WFV is an over 200 mV work function difference between (100) and (111) oriented grains of TiN and there is also an additional WFV due to the composition or nitrogen concentration of the TiN [36]. Although the grain size of the TiN at side wall of the fin is different from the planar portion, the transmission electron microscope (TEM) observation of the planar test structure reveals that the grain size of the sputter-deposited TiN is around 20 nm.

Figure 20 shows statistical $I_{\rm on}$ variation of the 100-nm-long $L_{\rm G}$ FinFETs extracted at a constant $V_{\rm G}$ ($V_{\rm G}$= 1 V) and at a constant overdrive ($V_{\rm G}$ = $V_{\rm th}$+0.65 V). Note that the $\Delta V_{\rm th}$ contribution to the $\Delta I_{\rm on}$ is cancelled out in the constant overdrive case. It is clear form Fig. 20 that the variation of the $I_{\rm on}$ is much higher for the constant $V_{\rm G}$ case. This strongly support that the $\Delta V_{\rm th}$ is the major source of the $I_{\rm on}$ variation. The small $I_{\rm on}$ variation in the constant overdrive case is due to the small μ, $R_{\rm p}$, and $T_{\rm ox}$ variation. This result indicates that if we can reduce the WFV of the TiN MG FinFET, the circuit performance can be improved. A selection of the gate material and an optimization of the gate formation process are therefore the key for improving the MG FinFET characteristics.

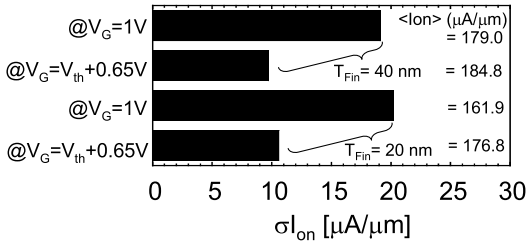

Fig. 20 Statistical ion variation of the 100-nm-long $L_{\rm G}$ FinFETs extracted at a constant $V_{\rm G}$ ($V_{\rm G}$ = 1 V) and at a constant overdrive ($V_{\rm G}$=$V_{\rm th}$+0.65 V).

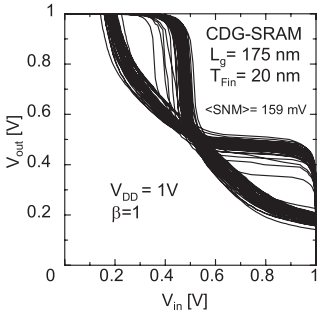

Fig. 21 Experimental butterfly curves of the common-DG FinFET SRAM cell.

4.2 SRAM Variation

These $V_{\rm th}$ and $I_{\rm on}$ variations will directly cause the variation in the SRAM performance. Fortunately, IDG-FinFET technology effectively controls of the $V_{\rm th}$ and thus can be used for the compensation of variability. In this section, variability of the CDG SRAM cell is compared with the Flex-PG cell. Moreover, experimental demonstration of the SRAM cell stability enhancement is shown using the IDG-FinFETs with the individual $V_{\rm th}$ controlling for the PG and the flip-flop (FF).

Experimental butterfly curves of the conventional CDG cell is shown in Fig. 21. The conventional CDG cell suffers from a marginal SNM due to the variation of the characteristics of the FinFET. To understand the appearance of the irregular curve in Fig. 21, characteristics of each transistor in the exactly same cell are measured. It is revealed that the irregular curves are due to the systematic variation in each FinFET. In this case, all the threshold voltages of the PG, PU, and PD are shifted negatively at the same time. This is explained by the WF lowering due to the composition or the thickness variation of the TiN gate. In addition, by correlating other butterfly curves with the IV characteristics of the FinFETs in each cell, it is concluded that the variation of the SRAM cell is due to the $V_{\rm th}$ variation caused by the WFV.

On the other hand, Fig. 22 shows the characteristics of the Flex-PG cell. The fixed bias for all the PG in the ac-

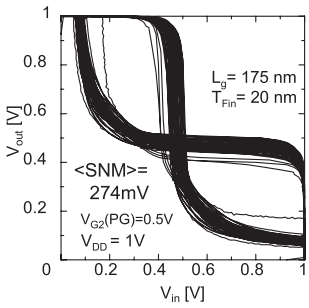

Fig. 22 Experimental butterfly curves of the Flex-PG FinFET SRAM cell.

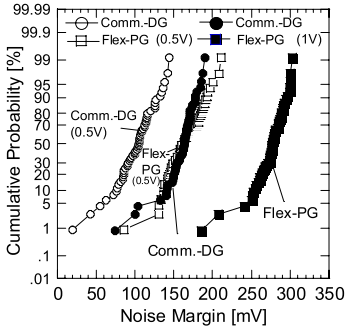

Fig. 23 Noise margin distributions of the CDG and Flex-PG cell during 1 V and 0.5 V operation.

cessed column is applied to reduce the drivability. In this case, V_{G2} is fixed at half of the V_{DD}. The V_{th} variation of the IDG-FinFET still exists, however, a significant enhancement of the SNM is clearly shown and an effect of V_{th} variation is decreased. The typical read current of the CDG cell is 11 μA, whereas that of the Flex-PG cell is 5 μA with the bias voltage (V_{G2}) of 0.5 V. Thus, there is a trade-off between the SNM enhancement and the read current. While in a writing operation, the V_{th} of PG can be lowered by the control terminal and the writing time can be shortened compared to the CDG cell.

Figure 23 shows the probability distribution of the noise margins. A 1.7x enhancement in the SNM is successfully demonstrated. It is also revealed that the statistical distributions of the noise margins of the CDG and Flex-PG cells are similar regardless of the operation voltage. This indicate that the average value of the SNM decreases with the same σ(SNM) when the VDD decreases.

4.3 Compensation of Variability in the SRAM Cell

To demonstrate how to cancel the SRAM variation after the fabrication, the experimental cell with the custom V_{th} tuning for the PG and the flip-flop (FF) for each cell is investigated. Firstly, the FF operation is harmonized so that the logical threshold of the FF keeps 0.5 V by controlling the bias for the second gate in each transistor. However, the variation due to the PG is still present. Secondary, the PG is harmonized by applying the bias voltage so that the Vo

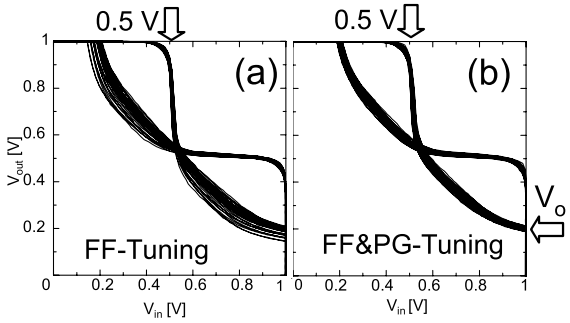

Fig. 24 Experimental reduction of the variation by tuning (a) the bias voltage for the flip-flop, and (b) both the bias voltages for the flip-flop and the pass-gate.

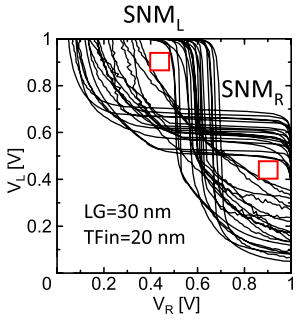

Fig. 25 Butterfly curves for the FinFET SRAM cells. Large variation of the SNM exists. SNM_L and SNM_R are defined depending on the two different memory states. The squares in the figure show worst case SNM_L and SNM_R.

keeps constant as shown in Fig. 24(b). As a results, SRAM characteristics become completely healthy and the smallest σ(SNM) is clearly demonstrated. These results indicate that not only the characteristics of the FF but also that of the PG needs to be independently harmonized to achieve the variation tolerant SRAM cell operation. This method cannot be directly applicable to the large scale of SRAM matrix, however, the area based FF/PG tuning with a reasonable number of control lines to decrease the systematic V_{th} variation may be a possible solution for the SRAM matrix.

4.4 Correlation of Variability in the SRAM Cell

In the previous section, the characteristics of the SRAM cell are harmonized by tuning the characteristic of each FinFET. However, it is not clear how the variation of the each transistor affects the variation on the SNM. In this study, to analyze the effect of the V_{th} variation on the SNM in detail, we define the SNM_L and SNM_R representing the static noise margins with the different memory state of the storage node L and R as shown in Fig. 25. Usually, the SNM of the SRAM cell is defined by taking the minimum between the SNML and the SNMR. In this study, the correlation between the variation in each transistor and the SNM is analyzed by determining the V_{th} of the pull-up (PU), pull-down (PD), and pass-gate (PG) transistors and the SNM_L and the SNM_R of each SRAM cell.

Figure 26 shows the effects of the V_{th} of each transistor

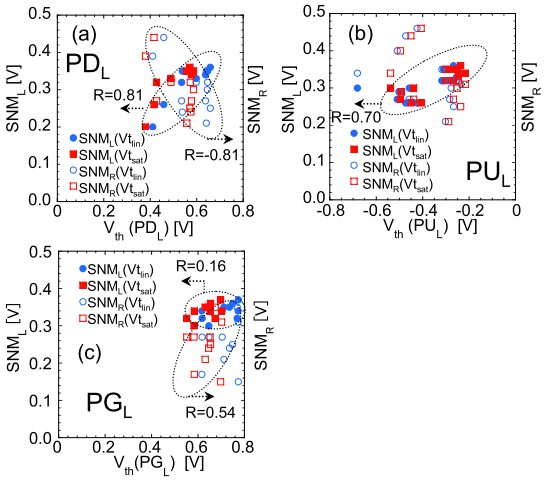

Fig. 26 Relationship between the SNMs and the V_{th} of the PD_L(a), PU_L (b), and PG_L (c).

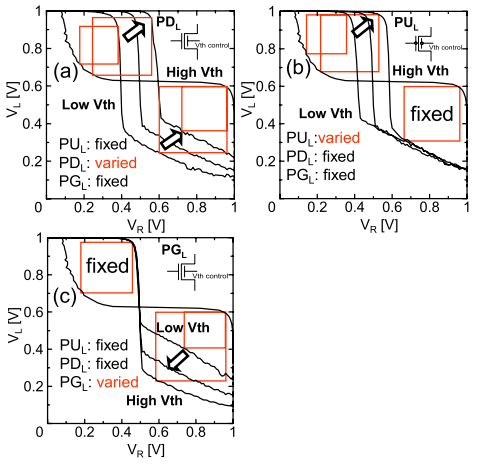

Fig. 27 Butterfly curves of the SRAM cell with the varied V_{th} of the PD_L (a), PU_L (b), and PG_L (c) by using the IDG-FinFET.

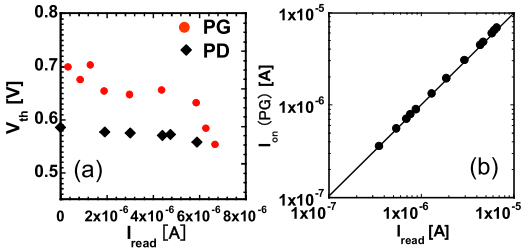

Fig. 28 (a) Relationships between the I_{read} and the V_{th} of the PG and PD. (b) Relationship between the I_{read} and the I_{on} of the PG. The read current is correlated with the V_{th} of the PG_L. A one to one relationship was revealed between the Ion of the PG and the I_{read}.

on the SNM_L and SNM_R. In this analysis, we focus on the transistors in node L. We reveal that the SNM_L has a positive correlation with the V_{th} of the PD_L and PU_L. On the other hand, the SNM_R has a negative correlation with the PD_L and a positive correlation with the PG_L. No correlation is found between the PU_L and the SNM_R and between the PG_L and the SNM_L. Thus, the V_{th} of each transistor correlates with the SNMs and the correlation is strongly dependent on the SRAM memory state. If we focus on the storage node R, on the other hand, the same correlation can also be found in the node R. These results are in accordance with the analytical expression of the SNM in the previous literature [37], since the varying the V_{th} of the FinFET affects the $r = \beta_{PD}/\beta_{PG}$ and the $q = \beta_{PU}/\beta_{P}G$ where β indicates the trans-conductance factor and thus positively or negatively correlates with the SNM.

To investigate the correlation further, we also take advantage of the independent-DG (IDG) SRAM technology. In Fig. 27(a), only the V_{th} of the PD_L is varied and that of the other transistors are fixed. In this case, the transfer curve of the SRAM cell splits into three lines by changing the PD_L from the low V_{th} to the medium and the high V_{th}. Thus, both the SNM_L and SNMR change and we reveal a positive correlation between the V_{th} and the SNM_L and a negative correlation between the V_{th} and the SNM_R. The transfer curve also shifts for the PU_L and PG_L cases. For the PU_L case, the transfer curves split and merge into the same line by increasing the V_R. This is caused by the difference in effectiveness of the PU_L to the node L and node R. Thus, the SNM_L increases with the V_{th} of the PU_L, however, the SNM_R does not shift. For the PG_L case, the transfer curves follow the same line and split into three lines. The SNM_R increases with the V_{th} of the PG_L and the SNM_L does not shift for the PG_L. These results completely coincide with Fig. 26. Thus, the correlation between the V_{th} and the SNM as shown in Fig. 26 is clearly explained by the shift in the transfer curves due to the V_{th} variation of the transistors. Moreover, the Flex-PG SRAM cell in the previous section uses this positive shift of the SNM by the PG_L. In Fig. 27, a tradeoff is found between the V_{th} of the PD_L and the SNM. Namely, the SNM_L increases with the V_{th} of the PD_L and the SNM_R decreases. No trade-off is found for the PU_L and PG_L cases. This indicates that V_{th} of the PD_L can be optimized to enhance SNMs.

Figure 28 shows the relationship between the read current (I_{read}), the V_{th} of the PG and PD, and the I_{on} of the PG_L. The I_{read} is correlated with the V_{th} of the PG_L. Also, one to one relationship is revealed between the Ion of the PG_L and the I_{read} due to the saturation mode operation of the PG_L. Thus in addition to the V_{th} variation, the Ion variation caused not only by the V_{th} variation but also by the R_{para} and the g_m variation is important since it directly modulates the read current.

Figure 29 shows the measured SNM from Fig. 27 as a function of the V_{th} of the PU_L, PD_L, and PD_L of the IDG-FinFET with various V_{th} by controlling the biasing gate. The correlation is completely reproduced by the IDG-FinFET technology. Moreover, the partial derivatives (∂SNM/∂V_{th}) which indicate the strength of the correlation can be calculated. As mentioned previously, the tradeoff exists between the V_{th} of the PD_L and the SNM. An optimal point can be clearly seen in Fig. 17(a) at V_{th} = 0.4 V.

To investigate the contribution of the V_{th} variation of

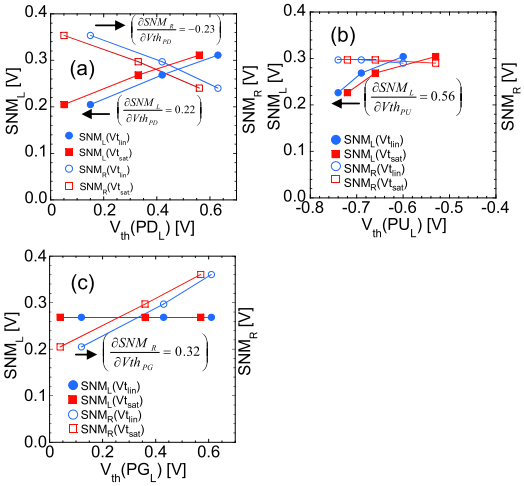

Fig. 29 The measured SNM as a function of the V_{th} of the PD_L (a), PU_L (b), and PG_L (c) taken by controlling the second gate of the IDG-FinFET. The slope represents sensitivity.

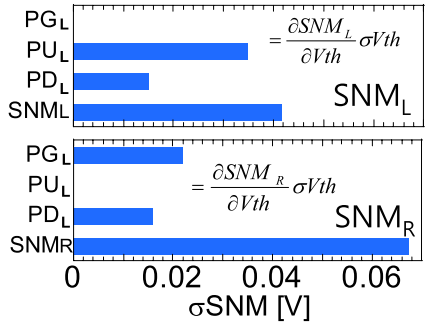

Fig. 30 Contribution of the V_{th} variation of each transistor to the σSNM.

each transistor to the σSNM as sensitivity analysis, we also rely on the following error propagation law (5) as used in Sect. 4.1.

$$(\sigma SNM)^2 = \sum_i \left(\frac{\partial SNM}{\partial Vth_i} \sigma Vth_i \right)^2 \quad (5)$$

Figure 30 compares the effect of each component by calculating $(\partial \mathrm{SNM}/\partial V_{th})^* \sigma V_{th}$. Strong correlations of the PG_L and PD_L to the SNM_R and PD_L and PU_L to the SNML are found. Also, contribution of each component to the σSNM and the severity of the variability in the different cell transistor are clarified. This indicates that the variability of each transistor should be individually tuned by considering its effect on the SNMs.

5. Conclusion

Multi-Gate device technology has been proposed for the enhancement of the device characteristics of the scaled MOSFETs. Moreover, independent-DG FinFET SRAM technology has been proposed for the enhancement of the SRAM characteristics. It is revealed that the read and write noise margins have been increased and the variability problem has been reduced thanks to the flexible V_{th} controllability. These results indicate the effectiveness of the independent-DG technology to enhance circuit performance.

Acknowledgments

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