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# 25-Gbps/ch Error-Free Operation over 300-m MMF of Low-Power-Consumption Silicon-Photonics-Based Chip-Scale Optical I/O Cores

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**SUMMARY** Aiming to solve the input/output (I/O) bottleneck concerning next-generation interconnections, 5 × 5-millimeters-squared silicon-photonics-based chip-scale optical transmitters/receivers (TXs/RXs)—called "optical I/O cores"—were developed. In addition to having a compact footprint, by employing low-power-consumption integrated circuits (ICs), as well as providing multimode-fiber (MMF) transmission in the O band and a user-friendly interface, the developed optical I/O cores allow common ease of use with applications such as multi-chip modules (MCMs) and active optical cables (AOCs). The power consumption of their hybrid-integrated ICs is 5 mW/Gbps. Their high-density user-friendly optical interface has a spot-size-converter (SSC) function and permits the physical contact against the outer waveguides. As a result, they provide large enough misalignment tolerance to allow use of passive alignment and visual alignment. In a performance test, they demonstrated 25-Gbps/ch error-free operation over 300-m MMF.

***key words:*** *Si photonics, low-power-consumption, small footprint, high density interface, I/O bottleneck*

## 1. Introduction

At present, optical interconnections in high-end servers and high-performance computers are in great demand because they can cover the long transmission distances that electrical interconnections cannot as data rates increase. Moreover, the electrical I/O bandwidth of the off-card and off-module used in data communication is approaching its limit [1]. To solve this I/O bottleneck, it is thus becoming practical to replace electrical interconnections with optical interconnections—even for shorter distances. To expand the off-card and off-module bandwidths using optical interconnections, high-speed, high-density, compact, low-cost, low-power-consumption, and reliable optical transceivers are needed. The features of silicon-photonics-based optical modules satisfy these requirements for the following reason: optical modules based on silicon photonics are commercially available. Silicon-photonics devices are suitable for low-cost mass production because they are produced on the fabrication line for conventional silicon electrical devices. Since the bending loss of silicon waveguides on silicon photonics is small, due to the large difference between the refractive indices of the core and cladding material, TX and RX devices with high-density photonics circuits have a small footprint. Moreover, these devices are reliable because they use technologically mature long-wavelength laser diodes. High-speed operations (over 25 Gbps) of silicon-photonics TX and RX devices have also been reported [2]–[4].

However, it is also important to enhance the efficiency of mass production by pursuing common ease of use of optical interfaces on printed circuit boards (PCBs) and in MCMs and optical modules. Common ease of use of these optical interfaces is achieved by employing low-power-consumption ICs, 1.3-μm MMF transmission, a user-friendly interface, and a compact footprint. MMF transmission at 1.3-μm wavelength is especially promising in regard to most conventional applications up to 300-m transmission distance at high speed, because a MMF with lower modal dispersion at 1.3-μm wavelength was developed [5], and the transmission distance in the case of that MMF is longer due to the minimum chromatic dispersion at this wavelength.

In this study, to satisfy the above-stated requirements, new silicon-photonics-based chip-scale optical TXs and RXs, called optical I/O cores, with 4-, 8-, or 12-channel I/Os for 25-Gbps/ch signal transmission, are proposed. By employing 1-V complementary metal oxide semiconductor (CMOS), the total power consumption of the TX ICs and RX ICs was 5 mW/Gbps. Moreover, the optical I/O cores have a small assembly size (5 × 5 $mm^2$) and include optical pins and TGVs (through-glass vias) or wire bonding pads as I/Os; consequently, their structures are suitable for high-density integration not only in conventional optical modules but also on PCBs and in MCMs. 25-Gbps/ch error-free transmissions through 300-m MMF in the O band between the TX and RX of the developed optical I/O cores was achieved.

## 2. Target Specifications

Several applications of optical I/O cores, for example, as optical engines of active optical cables (AOCs) and on-board modules and as optical interfaces in application-specific integrated circuits (ASICs) and field programmable gate array (FPGA) packages, are expected.

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The prototypes of AOCs are shown in Fig. 1. To achieve a low-cost module, fiber connectors must be mounted on the optical I/O cores by passive alignment or visual alignment. To apply such alignment techniques, as a multi-mode waveguide, a transmission medium like a GI50 MMF is indispensable because it has a large alignment tolerance in regard to the optical components. On the other hand, the AOC must cover a transmission distance of over 300 m to meet the requirements concerning data centers.

An image of an MCM with an ASIC or FPGA chip is shown in Fig. 2. The optical I/O cores must have a small footprint and high-density I/O because they are mounted on the same interposer with the ASIC or FPGA chip. Moreover, the power consumption of the optical I/O cores must be suppressed, since they are located close to the heat-generating ASIC or FPGA chip.

In consideration of these applications, the target specifications of the optical I/O cores were determined as listed in Table 1. The target data rate per channel ranges from 25 to 28 Gbps. Both the TX and RX are 5×5 mm$^2$ in size and have 4-, 8-, or 12-channel I/Os. 1-V CMOS circuits (driver and transimpedance amplifier, TIA) were developed and used for the TX and RX ICs to achieve low-power-consumption operation. The target power consumption per data rate of ICs was designed to be 5 mW/Gbps. The driver and TIA are basically driven at 0.9 V. A supply voltage of 3.3 V is applied to control the modulator bias and photodiode (PD) bias. The wavelength of the light sources is 1.3 µm, and the transmission medium is MMF.

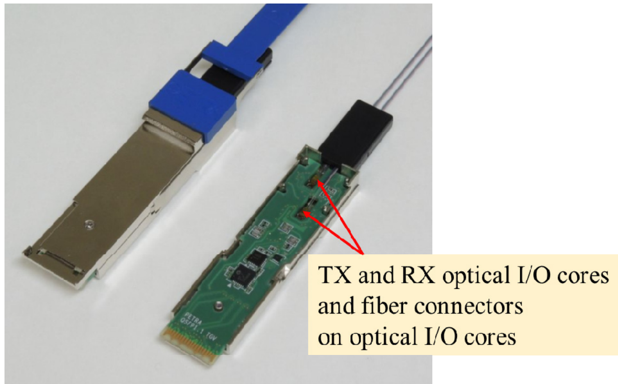


**Fig. 1** Prototypes of AOCs.

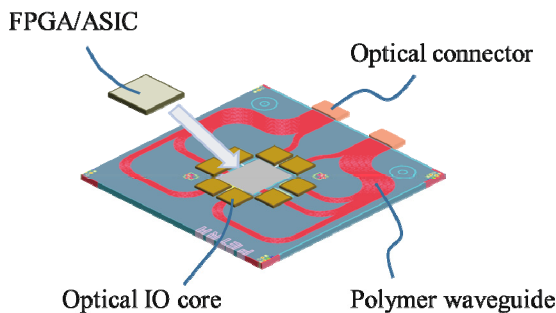


**Fig. 2** Image of MCM with ASIC or FPGA chip.

## 3. Structures of Optical I/O Cores

### 3.1 Optical I/O Core and Its Constituent Elements

Photographs of the TX and RX 4-channel × 25-Gbps parallel optical I/O cores are shown in Figs. 3 (a) and (b), and their cross sections are shown in Figs. 4 (a) and (b).

The optical I/O core basically consists of a silicon-photonics platform, optical pins, a cover glass, a CMOS IC (driver or TIA), and decoupling capacitors. In addition

**Table 1** Target specifications of optical I/O core.

| | |
|---|---|
| Data rate | 25-28 Gbps/ch |
| Size | 5 mm × 5 mm |
| Number of channels | 4 or 8 or 12 |
| IC power consumption | 5 mW/Gbps |
| Power-supply voltage | 3.3 V/0.9 V (TX)<br>3.3 V/0.9 V (RX) |
| Wavelength | 1.3 µm |
| Transmission medium | MMF |

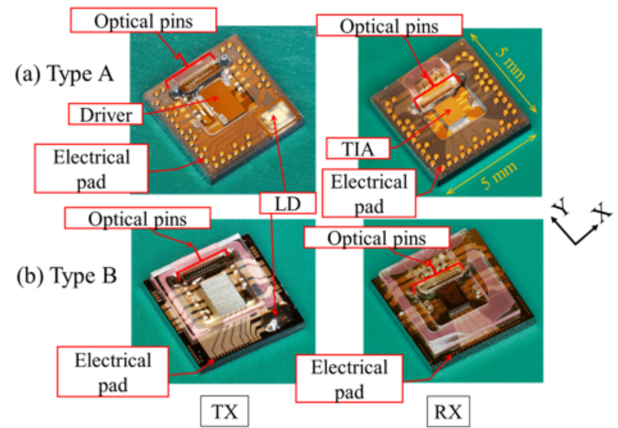


**Fig. 3** Photographs of TX and RX 4-channel × 25-Gbps parallel optical I/O cores.

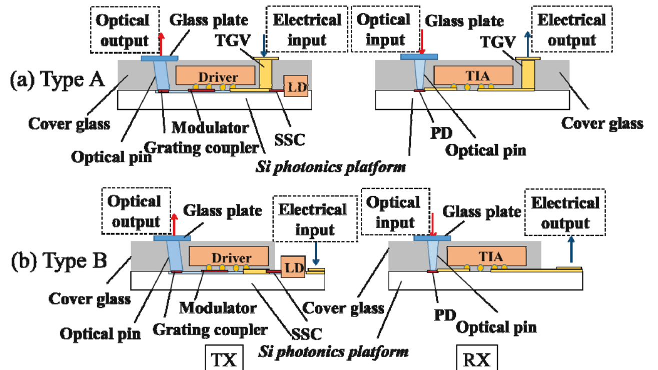


**Fig. 4** Cross sections of optical I/O cores.

to these components, 1.3-μm Fabry-Perot laser diodes (FP-LDs) integrated with SSCs are mounted in the TX as a light source. Two types of optical I/O cores (regarding their electrical interfaces) were fabricated: "type A" (with a structure to be flip-chip mounted in the package) and "type B (with a structure for wire bonding). As for type A, TGVs are formed in a cover glass, and the electrical pads are formed on the surface of the glass. On the other hand, as for type B, the electrical pads are arranged on the periphery of a silicon-photonics platform. The direction of the optical interface can be changed when it is mounted by selecting the device structure as type A or type B.

### 3.2 Silicon-Photonics Platform

The TX silicon photonics platform includes SSCs [7] for coupling the output from the FP-LDs, Mach-Zehnder modulators with metal-oxide-semiconductor (MOS)-type optical phase shifters, grating couplers (GCs) for extracting the optical signal from the silicon-photonics devices, and electrical signal lines for the driver. The RX silicon-photonics platform includes surface-illuminated 30-μm-ϕ Ge PIN photodiodes and electrical-signal lines for the TIA. The input-signal lines in the TX and the output-signal lines in the RX are both differential coplanar waveguides with 100-Ω characteristic impedance.

### 3.3 Mach-Zehnder Modulator

Each of the Mach-Zehnder modulators is structured with a tiny, linear-accelerator in-line centipede electrode [6]. The optical waveguide with a MOS junction was divided into four segments in accordance with the electrode pitch. The resulting four divided MOS junctions were individually driven by differential outputs of the driver with delay tuned in accordance with the optical-propagation delay. The length and number of segments were adjusted so that the capacitance of each MOS junction was low enough to be driven at high-speed by the driver while keeping power consumption sufficiently small.

### 3.4 Driver and TIA

The driver and the TIA were fabricated using 28-nm CMOS process technology. The driver has a differential input and four differential outputs per channel, which drove the divided segments in the Mach-Zehnder modulator. The driver consisted of a current-mode-logic (CML) input buffer and CMOS inverters. The power consumption per data rate of the driver was designed to be 3.1 mW/Gbps. The differential output-voltage swing of the driver was 1.8 Vp-p. The TIA consists of a transimpedance amplifier using a CMOS inverter, CML limiting amplifiers, and a CML output buffer. The differential output-voltage swing of the TIA is controlled from 580 to 970 mVp-p according to application by changing the supply voltage for the output buffer from 0.7 V to 1.1 V. Minimum power consumption per data rate of the TIA was 1.8 mW/Gbps.

### 3.5 Optical I/Os

The optical interface consists of an array of vertical polymer multimode waveguides called "optical pins" [9]. Each optical pin consists of a core and a cladding using two types of ultraviolet (UV) curable resin. The optical pins can be formed on the silicon-photonics platform using a photolithographic technique. The height of the optical pins, which can be adjusted to the height of the cover glass, is 300 μm. To keep the height constant, a glass plate with thickness of 50 μm is arranged over the optical pins before they are fabricated. The height of the cover glass is higher than the height of the hybrid-integrated IC. As a result, the driver and the TIA are protected in the cover glass, and physical contact between the outer waveguides and the optical pins are facilitated.

Using these pins makes it possible to form the PDs in close vicinity to the hybrid-integrated TIA and, thereby, reduce signal loss. The pitch of the pins as the optical interface is 250 μm at present; however, the feasibility of optical pins with pitch of less than 125 μm has been confirmed.

Moreover, the optical pins can be formed with a tapered shape and a tilt angle by tuning the UV exposure condition [8]. By applying the taper shape, beam size of the incident light can be controlled, and misalignment tolerance against the outer waveguides can be optimized. In the RX, the core size of the optical pins on the outer-waveguide side is set to 70 μm-ϕ to collect the light from the GI50 MMF. To illuminate the small photosensitive area of the PDs, the core size (diameter, ϕ) on the silicon-photonics platform side was set to 30 μm. In the TX, the core size of optical coupling pin was set 35 μm, and the tilt angle was set to 8 degrees in accordance with the output angle from the GC. By applying the tilt angle, beam-divergence angle is kept small, and generation of higher-order propagation mode at the optical pins is suppressed.

### 3.6 Electrical I/Os

In the type-A optical I/O cores in Fig. 3 (a), the pads on the cover glass with the TGV are electrical interfaces, where the minimum pad pitch is designed to be 350 μm. In consideration of flip-chip mounting on the interposer or the PCBs, electrical I/O pads can be placed not only on the periphery of the optical I/O core chips but also in the inside area, thereby making the most of the TGVs. It is therefore easy to increase the number of electrical I/O pads for multi-channel devices while keeping the pad pitch constant. Employing the TGVs means that the necessary area for mounting and connecting the electrical I/Os to the pads on the interposer or the PCBs becomes smaller than when wire bonding is used. Moreover, the type-A optical I/O cores are suitable for mounting on the optical-waveguide-integrated interposer or PCBs because the height of the electrical I/Os is the same as that of the optical I/Os and both I/Os can be connected at once.

In the type-B optical I/O cores shown in Fig. 3 (b), the electrical I/O pads are arranged on the silicon-photonics platform. After mounting and wire bonding optical I/O cores, the direction of the optical interface is opposite to that in the type-A optical I/O cores. Accordingly, with the type-B the optical I/O cores, the optical I/Os can be handled independently of the electrical I/Os. It is also possible to assemble an optical connector after the optical I/O core chip is mounted on the interposer or the PCBs.

### 3.7 Assembly Process

The optical I/O cores were fabricated as follows. After the silicon-photonics platforms were fabricated by using a silicon-wafer process, the LDs and ICs were mounted using passive alignment and micro flip-chip bonding. The cover glass was then laminated on the surface of the silicon-photonics wafer. Finally, the optical pins were formed. Because of their flat structure, it is possible to use a wafer-level packaging process and test operation at wafer level, thereby reducing assembly and test costs.

## 4. Coupling Characteristics Using Optical Pins

### 4.1 Estimation of Misalignment Tolerance by Using Ray Tracing

Misalignment tolerance of optical coupling in relation to the optical pins was estimated as follows. The connection from the GC to GI50 MMF through the optical pin in the TX and the connection from the GI50 MMF to the photodiodes through the optical pin in the RX are shown in Fig. 5. It was assumed that these connections using the optical pins are "lensless". This type of connection is superior than that using a lens [11] because alignment tolerance in the two-axis that is perpendicular to the optical axis is just required, and the optical-axis tolerance can be ignored. On the other hand, controlling the beam-divergence angle is difficult in a lensless system. However, in the case that two types of multimode waveguides with different numerical apertures (NAs) are connected [12], the coupling loss becomes small by satisfying the following two requirements. One is that beam-divergence angle from the input waveguide is smaller than the NA of the output waveguide; another is that the input beam size is smaller than the core size of the output waveguide. The GC has a narrow beam-divergence angle and small beam size, so it is ideal for a lensless optical-link system.

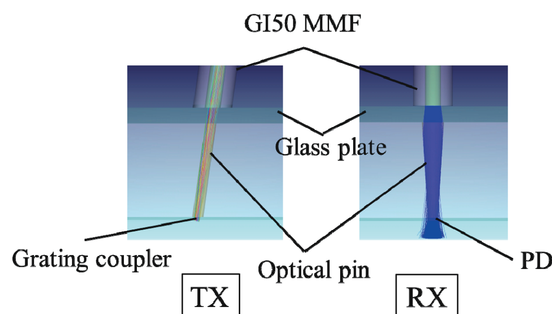


**Fig. 5** Connections between optical I/O cores and GI50 MMFs.

Ray tracing was used to estimate the misalignment tolerance. The coupling loss was calculated from an intentional displacement at the each connection. The coupling tolerance was estimated under allowable excess loss of 0.5 dB.

As for the TX side, the coupling loss from the GC to GI50 MMF was calculated. The input-light source consists of the aggregation of point sources reflecting the near-field pattern (NFP) and far-field pattern (FFP) of the GC. The NFP and FFP were calculated using finite-difference time-domain (FDTD) simulation. In Fig. 6, calculated NFP and FFP of the GC are shown. The GC is fan shaped, and the NFP reflects that shape. The spot size was less than 14 µm. The beam direction from the GC was designed to be inclined at 12.7° from perpendicular in air. The FWHM of the beam-divergence angle was less than four degrees. The x- and y-directions shown in Fig. 6 are the same as those shown in Fig. 3.

As for the RX side, the coupling loss from the GI50 MMF to the PD was calculated. The NFP and FFP of the input-light source into the GI50 MMF are shown in Fig. 7. This input field satisfies the over-filled-launch (OFL) condition. To suppress the leakage of the light over the core-cladding interface of the optical pins, a combination of available materials with a maximum difference in refractive in-

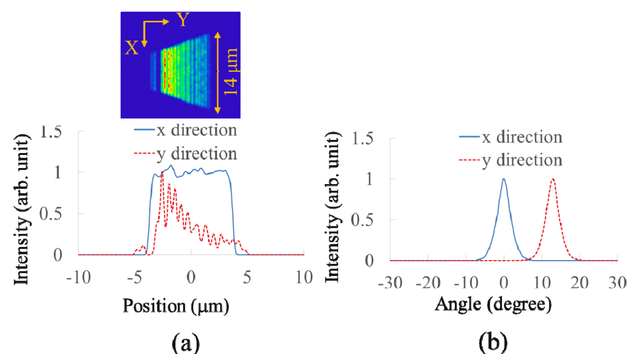


**Fig. 6** (a) NFP and (b) FFP of grating-coupler output model.

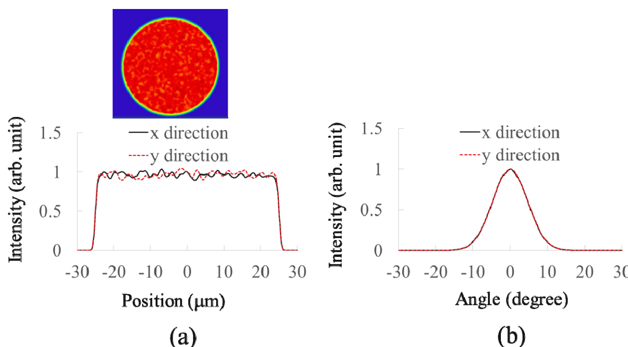


**Fig. 7** (a) NFP and (b) FFP of GI50 MMF input model.

dices was chosen. The refractive index difference Δ was 4.3%.

### 4.2 Calculation of Misalignment Tolerance

Calculated coupling loss at the TX side is plotted against misalignment between the GC and the optical pin (35-µm diameter) in Fig. 8. According to the figure, coupling tolerance between the GC and an optical pin is larger than 21 µm.

The tolerance at the RX side for misalignment between a photodiode and an optical pin is shown in Fig. 9. According to the figure, large coupling tolerance (more than 10 µm) is anticipated. Dependence of coupling loss on Δ at the RX side is plotted in Fig. 10. This figure confirms that leakage of light decreases as Δ increases.

Since the optical pins are formed using a photolithographic technique with accuracy of less than a few micrometers, the above-stated misalignment tolerance is wide enough to fabricate the optical pins.

Calculated coupling loss due to misalignment between the GI50 MMF and the optical pin (whose core diameter was 35 µm) at the TX side is plotted in Fig. 11. According to the figure, coupling tolerance between a MMF and an optical pin is larger than 26 µm.

The coupling tolerance between a GI50 and an optical pin whose core diameter is 70 µm at the RX side is shown in Fig. 12. Large coupling tolerance of more than 31 µm was anticipated.

There is the glass plate of 50 µm thickness on the optical pin and that is the free space where the beam will spread. However, in the TX side, the coupling loss was suppressed due to the small beam divergence angle of the light from GC. In the RX side, the coupling loss was suppressed due to the 70 µm core diameter and high Δ of the optical pin.

The optical pins must be connected with GI50 MMF using visual alignment method or passive alignment method with positioning pins and holes as the user-friendly inter-

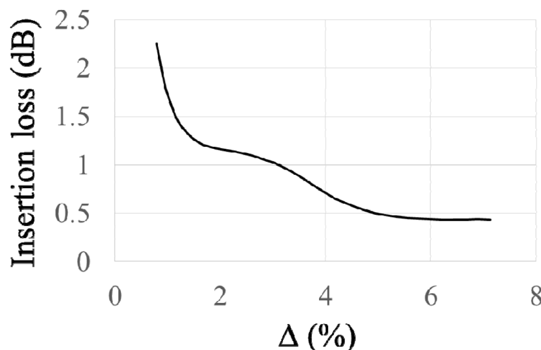


**Fig. 10** Dependence of coupling loss on Δ.

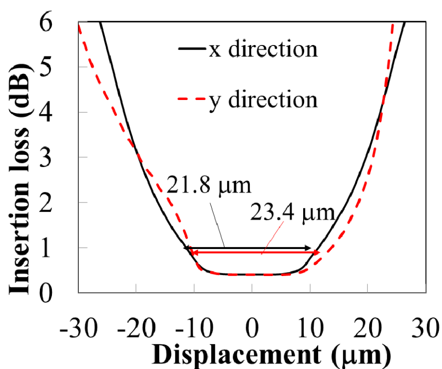


**Fig. 8** Calculated coupling loss between GC and optical pin.

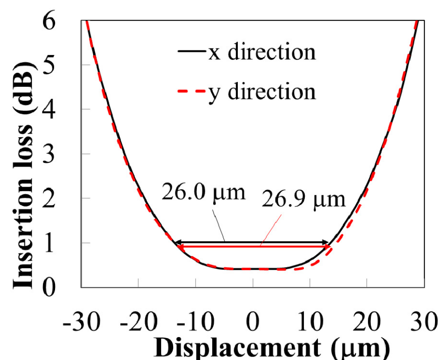


**Fig. 11** Calculated coupling loss of misalignment between GI50 MMF and optical pin on TX side.

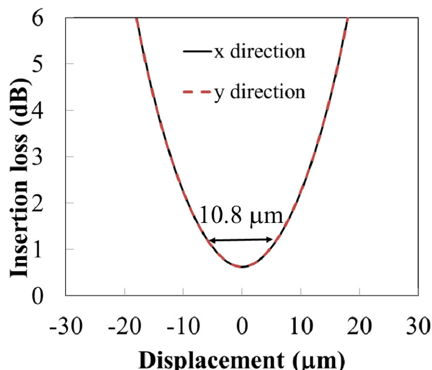


**Fig. 9** Calculated coupling loss between optical pin and photodiode.

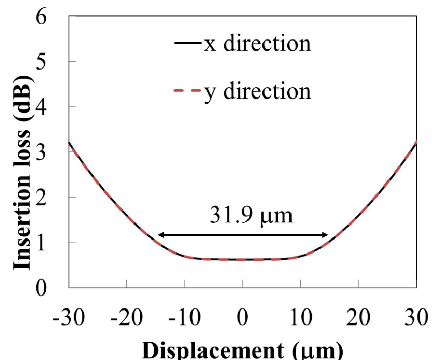


**Fig. 12** Calculated coupling loss of the misalignment between GI50 MMF and optical pin on RX side.

face. Misalignment tolerance of over 10 µm, preferably 20 µm, is necessary. Enough alignment tolerance between GI50 MMF and the optical pins was expected to be obtained.

### 4.3 Fabricated Optical Coupling Pin and Loss Measurement

The fabricated optical pins of the TX and RX are shown in Figs. 13 (a) and (b), respectively. 12 optical pins are standing in line at 125-µm pitch. The optical pins near both ends have a different shape due to shortage of the UV exposure amount. Channels ch1, ch2, ch11, and ch12 can be considered additionally fabricated dummy pins. An RX optical pin as seen from above is shown in Fig. 13 (c). Thanks to the glass plate, the surface of the optical pin is flat.

Dependence of core size of the (a) TX and (b) RX optical pin on core position is plotted in Fig. 14. According to the figure, core diameter varies with core position. Core diameters on the MMF side and the GC surface of the TX optical pins are 40 µm and 29 µm on average, respectively.

The measured diameter of RX core pins increases linearly from the silicon-photonics platform side. The respective core diameters on the MMF side and PD side are 68 µm and 26 µm on average, respectively. It is thus concluded that the RX optical pins were successfully fabricated according to the design described in the previous section.

Measured displacements of the TX and RX optical pins are shown in Figs. 15 (a) and (b). The actual displacements for the TX optical pin from ch3 to ch10 except dummy pins were less than 5.6 µm on the MMF side and less than 4.5 µm on the GC side. The values for the RX optical pin (except ch5) were less than 2.4 µm on the MMF side and less than 3.3 µm on the GC side. The large displacement of ch5 occurred in the rinse process. This can be improved by optimizing the rinse condition.

The measured and calculated coupling losses due to the misalignment between the GI-50 MMF and the TX optical pin are shown in Fig. 16 (a). The gap between the GI50 MMF and glass plate on the optical pin was 10 µm, which was filled with index matching oil for the measurement. The measured minimum coupling loss was 0.49 dB. The alignment tolerance was 10 µm, which is smaller than the calculated one but satisfies the tolerance needed for low-cost alignment.

The measured and calculated coupling loss due to the misalignment between the GI-50 MMF and RX optical pin is plotted in Fig. 16 (b). The dependence of measured coupling loss on displacement is similar to the calculated results. The measured minimum coupling loss was 0.41 dB, and the coupling tolerance is expected to be approximately 34 µm. According to this result, the actually fabricated op-

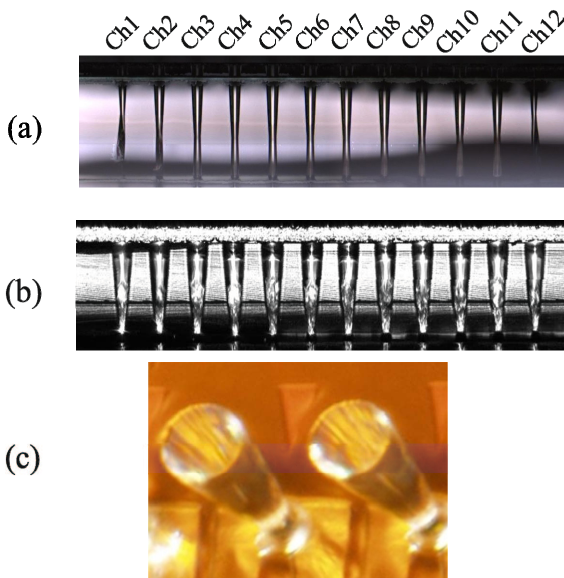


**Fig. 13** Photographs of fabricated optical pin of (a) TX, (b) RX and (c) top view of RX optical pins.

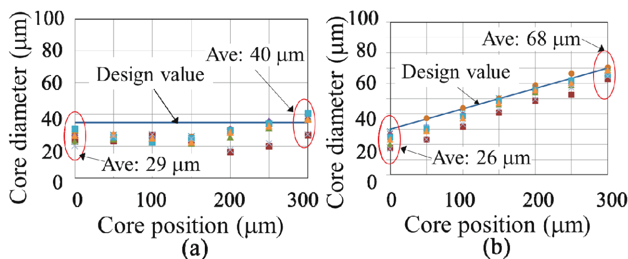


**Fig. 14** Dependence of core size of (a) TX and (b) RX optical pins on core height.

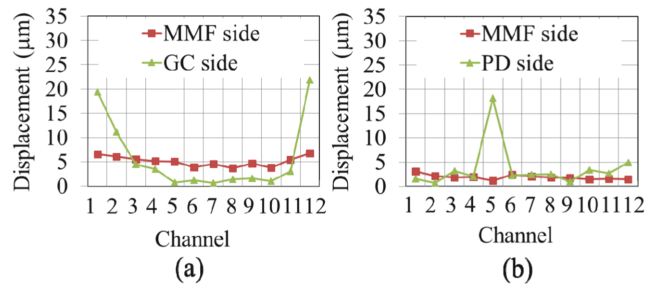


**Fig. 15** Measured displacement of (a) TX and (b) RX optical pins.

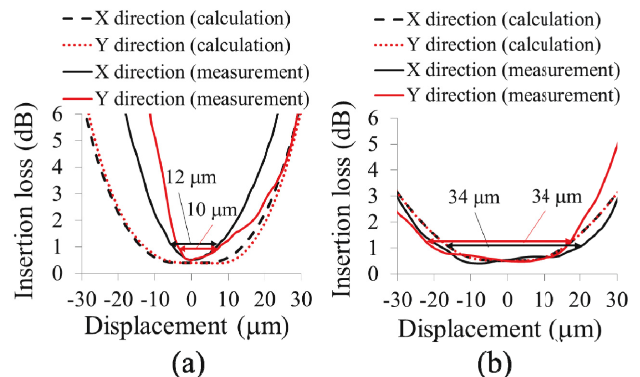


**Fig. 16** Measured and calculated coupling loss due to the misalignment between GI-50 MMF and optical pin on TX side (a) and RX side (b).

tical pin had enough misalignment tolerance to achieve a user-friendly interface.

## 5. Performance Test

### 5.1 Encircled Flux

To secure the MMF bandwidth for 850-nm vertical cavity surface emitting lasers (VCSELs) in the 10-Gb/s Ethernet standard, the launch condition determined by the encircled flux (EF) must be satisfied. With a 1.3-μm band optimized MMF, EF within 4.5 μm must be less than 30%, and EF within 19 μm must be more than 86%. Measured EF of the TX optical I/O core is shown in Fig. 17. EF was measured under the condition that the GI50 MMF is directly connected with the optical pin. The EFs within 4.5 μm and 19 μm met the required launch condition.

EF tolerance regarding misalignment between the optical pin and MMF was also measured. Dependences of EF within 4.5 μm and 19 μm for displacements in the (a) x- and (b) y-directions, respectively, are plotted in Fig. 18. EF within 4.5 μm is always less than 30%. Only EF within 19 μm shows a restriction regarding the displacement. The tolerance in the x-direction was 44 μm, and that in the y-direction was 24 μm. However, these tolerances were wider than the tolerance for the coupling loss. Accordingly, it can be concluded that the misalignment between the MMF and the optical pin was limited by its coupling loss.

### 5.2 Transmission Characteristics

To test the performance of the optical I/O cores, the 25-Gbps transmission characteristics with Corning Clearcurve® LX MMF were evaluated. TX and RX optical IO cores of the type-B were mounted on printed circuit boards for the evaluation. Three MMFs, 100, 300, and 500 m in length, were used for the test. The transmission rate was 25.78125 Gbps. TX optical eye patterns and RX electrical eye patterns after MMF transmission are shown in Figs. 19 (a) and (b), respectively. A pseudo random binary sequence (PRBS) pattern of $2^{31} - 1$ was applied. Clear eye openings were obtained up to 300 m. The TX eye pattern shows large inter-symbol interference (ISI) after 500 m. The extinction ratio of the TX back-to-back (B-to-B) eye pattern was 9.5 dB. The rise time and the fall time at 20%–80% were respectively 13.5 ps and 12.3 ps.

Dependence of deterministic jitter (DJ) and random jitter (RJrms) on misalignment between the MMF and the optical pin is plotted in Fig. 20. According to the figure, DJ and RJrms are significantly suppressed. This result coincides with the fact that EF had a wide misalignment tolerance. Bit error rate (BER) characteristics, including B-to-B transmis-

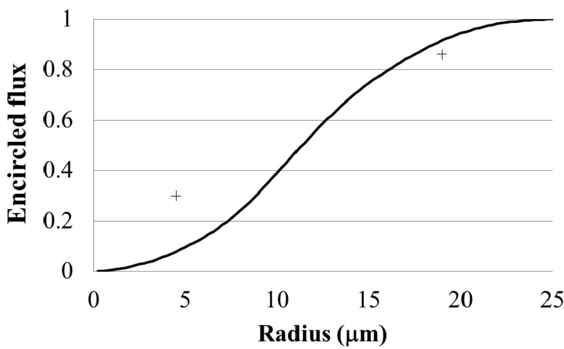


**Fig. 17** Measured EF of TX optical I/O core.

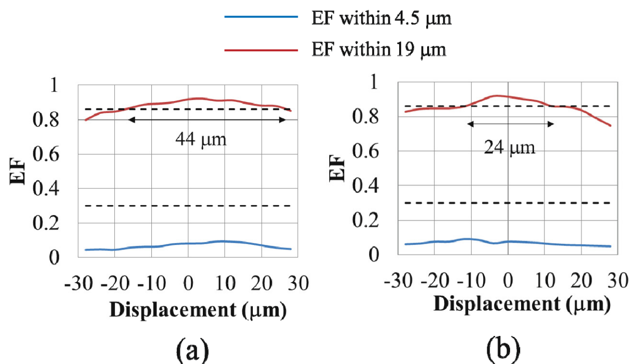


**Fig. 18** EF tolerance of the TX optical I/O core for displacement between MMF and optical pin.

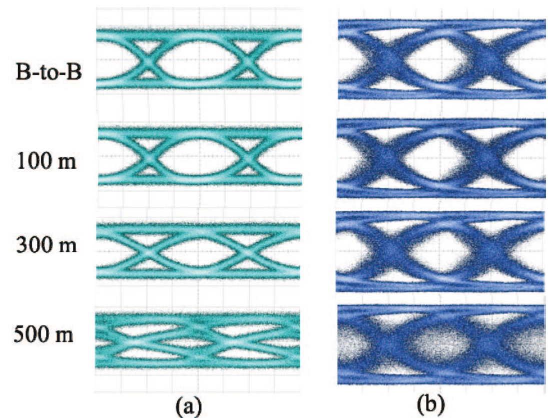


**Fig. 19** (a) TX optical eye patterns and (b) RX electrical eye patterns.

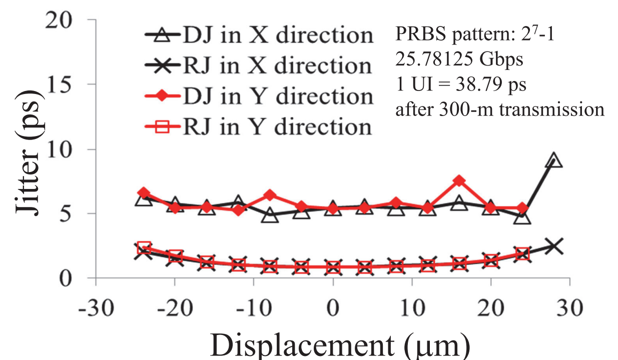


**Fig. 20** Dependence of deterministic jitter (DJ) and random jitter (RJrms) on misalignment between MMF and optical pin.

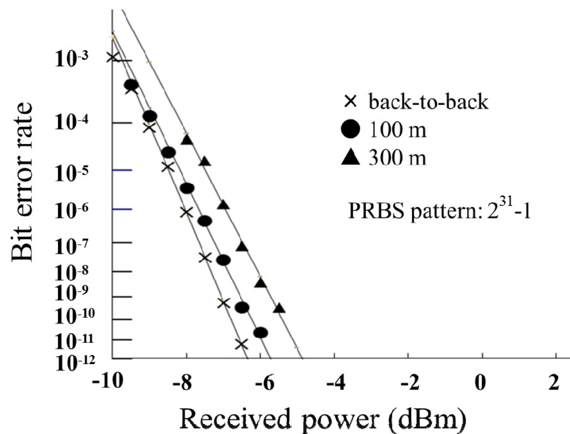


**Fig. 21** BER characteristics.

sion between the TX and RX, are shown in Fig. 21. According to the figure, error-free operation was obtained up to 300 m. The power penalty after 300 m transmission was 1.7 dB. The minimum average received power of B-to-B transmission is −6.3 dBm. These basic-performance results indicate that optical I/O cores are applicable to an interconnection covering a distance over 300 m (namely, that needed in a data center). Although results for the type-B optical I/O cores only are shown here, good eye openings (up to 300-m transmission) for the type-A optical I/O cores [10] were also obtained.

## 6. Conclusion

Called "optical I/O cores," hybrid-integrated low-power-consumption chip-scale optical TXs/RXs were developed. The power consumption of their hybrid-integrated ICs was 5 mW/Gbps. They demonstrated 25-Gbps/ch error-free operation over a 300-m MMF in the O band. The developed optical I/O cores can be used to provide next-generation interconnections for information technology (IT) systems and high-performance computers because of their common ease of use, low power consumption, low cost, high speed, high density, compactness, and reliability.

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