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FOREWORD

Special Section on Analog Circuit Techniques and Related Topics

The fifth-generation technology standard for broadband cellular networks, 5G, has been launched worldwide this year. 5G will provide unbeatable speeds, low-latency connectivity, and multiple connections simultaneously, therefore, its benefit will spread not only telecommunication, but also living, medical, automotive, and green technologies. On the other hand, the big data in cyberspace that accumulated the various information in physical space will be processing by AI. Hence, AI is one of the most promised technologies. Therefore, it is predicted to realize a smart society near the future, by these technologies. To develop the mentioned technology, it is necessary to the evolution of electronic circuits, such as digital and analog integrated circuits, especially the research and development of the analog integrated circuit is the most challenging work since all of the human interfaces are analog.

It is my pleasure to publish this special section, "Analog Circuit Techniques and Related Topics" this time. This special section consists of one invited paper and five regular papers. The invited paper entitled "A 26-GHz-Band High Back-Off Efficiency Stacked-FET Power Amplifier IC with Adaptively Controlled Bias and Load Circuits in 45-nm CMOS SOI", presents highly-linear millimeter wave power amplifier suitable for 5G communication with adaptive controlled bias and load circuits using Si SOI CMOS process, which is very helpful to realize high efficiency power amplifier.

The five regular papers include subjects of AM-AM/PM characterization of a HBT power amplifier, low-power LNA for 3D ultrasound beamformers, short startup time and low temperature coefficient on chip oscillator, low-voltage low-power intermittent start-up circuit for energy harvesting, a novel digital calibration algorithm for SAR-ADC circuit. These novel technologies will be great help for all of the readers.

On behalf of the editorial committee of this special section, I would like to express our sincere appreciation to all the authors of the submitted manuscripts and all the reviewers for their great contribution and helpful effort. I also would like to thank all of the committee members for their valuable efforts in this editorial work. Finally, I would like to express my special thanks to Dr. Yoshiaki Yoshihara, Prof. Kazuyuki Wada, and Dr. Junya Matsuno for their hard works as secretaries and liaison.

Nobuyuki Itoh, Guest Editor-in-Chief

Nobuyuki Itoh *(Senior Member)* received the B.S. and the M.S. degrees in chemistry from Tokyo University of Science, Tokyo, Japan, in 1983 and 1985 respectively, and the Ph.D. degree in physical electronics from Tokyo Institute of Technology, Tokyo, Japan, in 2006. In 1985, he joined the research and development center, Toshiba Corporation, Kawasaki, Japan, where he was engaged in the research and development of CMOS device technologies, bipolar device technologies, bipolar circuits design and RFCMOS circuit design. He had been a visiting scientist at Katholieke Universiteit Leuven, ESAT-MICAS, Leuven, Belgium, from 1996 to 1998, where he had worked on design of fully integrated VCOs and PLLs using RFCMOS. He has been engaged in the research and development of high-frequency analog circuit at Semiconductor Company of Toshiba Corporation since 1998. He was also a part-time lecturer of Chuo University, Tokyo, Japan, for 2009 to 2010. Since 2010, he has been full time professor of Okayama Prefectural University. His current research interests are high-frequency integrated circuit for telecommunications. Dr. Itoh is a member of IEEE and also senior member of IEICE. He received the Asia-Pacific Microwave Conference (APMC) Prize in 2007. He has been a member of TPC of CICC, BCTM, ESSCIRC, RFIC, APMC, and RFIT, was a secretary of IEEE MTT-S Japan Chapter, was the Publicity Chair of APMC 2010, and was a secretary of URSI-C Japan Committee.