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Kikai-Shinko-Kaikan Bldg., 5-8, Shibakoen 3 chome, Minato-ku, TOKYO, 105-0011 JAPAN

PAPER

Maximum Output Power Design on an 85kHz Class-D Half-bridge ZVS Inverter with Power-MOSFETs

Yi XIONG[†], ***nonmember,*** **Senanayake THILAK**[†], ***nonmember,*** **Daisuke ARAI**[†], ***nonmember,***
Jun IMAOKA[†] ***member,*** **Masayoshi YAMAMOTO**[†] ***member***

SUMMARY ***This paper analyzed and verified the condition for obtaining the maximum output power with an 85kHz class-D half-bridge zero-voltage-switching (ZVS) inverter. The shunt capacitance in the class-D half-bridge ZVS inverter is formed by nonlinear parasitic capacitance and linear external capacitors. The design equation of the shunt capacitance is derived. For verification, two class-D half-bridge inverters are designed with Si-MOSFETs and SiC-MOSFETs in four specifications. The simulated and experimental waveform verified the validity of the design procedure for achieving the ZVS operation, and the measured result verified the analysis of output power characteristics with good consistency. Furthermore, the relationship between the maximum output power and parasitic capacitance is analyzed. It is clarified that the power MOSFET with smaller parasitic capacitance can obtain higher maximum output power. By comparing the maximum output power between the Si-MOSFET and SiC-MOSFET, it is indicated that the SiC-MOSFET with smaller parasitic capacitance can obtain higher maximum output power than Si-MOSFET, verifying the condition for obtaining the maximum output power.***

Keywords: 85kHz, class-D half-bridge inverter, ZVS, maximum output power, Si-MOSFET, SiC-MOSFET.

1. Introduction

The class-D inverter [1–13] is a well-established circuit excelling in converting DC power to AC power. With the advantage of low voltage stress to the power device, the class-D inverter finds wide applications in DC-DC resonant converters [7], induction heating [8], induction lamp [9], radio transmitter [10], and wireless power transfer (WPT) [11-13]. There are two topologies in class-D inverters: the half-bridge type [14] and the full-bridge type [15]. The half-bridge type contains only two switches, resulting in lower conduction loss, switching loss, and switching noise than the full-bridge type. Additionally, it offers advantages in industrial design such as smaller size, lighter weight, and lower production cost.

The WPT for electric vehicle (EV) battery charging has become a focal point of research [16-18]. The power transmitter is typically installed in a confined space under the ground and operates in high ambient temperatures [19]. Moreover, the communication system between the transmitter and receiver requires a low electromagnetic interference (EMI) environment [20-21]. Thus, it can be inferred that the class-D half-bridge inverter, with its features of low power loss, low noise, and compact size, is more suitable for the EV WPT system. The Society of Automotive Engineers (SAE) International has selected an operating frequency band of 85kHz for EV WPT [22-23], allowing the class-D half-bridge inverter to operate with power devices such as Si-MOSFETs and SiC-MOSFETs [24], etc.

However, due to having only two switches, the class-D half-bridge inverter outputs only half of the DC input voltage, limiting the output power. To maximize the output power, firstly, the zero-voltage-switching (ZVS) operation is necessary to reduce the energy loss [25-32]. With the ZVS operation, low switching loss can be achieved, thereby reducing the heat dissipation of the power device, and maintaining normal ambient temperature. Thus, the on-resistance will not increase due to the temperature characteristic, indirectly omitting the additional conduction loss. Secondly, under the ZVS condition, all power-related parameters need to be optimized to maximize the output power. To facilitate the design process, the output power characteristic under the ZVS condition needs to be analyzed. Therefore, an analytical model encompassing all power-related and ZVS-related parameters.

In [25], an analytical model for designing the class-D ZVS inverter was developed without considering the nonlinear parasitic capacitance. The nonlinear parasitic capacitance cannot be removed from the practical power device. Designing the shunt capacitance accurately through this model to satisfy ZVS conditions is challenging, leading to the failure of ZVS operation in practical circuits. On the other hand, output power characteristics were analyzed under the ZVS condition, indicating that high output power can be achieved with a 0° output current phase angle (class-DE mode), large duty, and high DC input voltage. However, in verification, no output power was measured in class-DE mode, and the measured results did not validate the output power characteristics.

In [32], an analytical model for designing the class-D ZVS inverter was developed with consideration of the nonlinear parasitic capacitance. The frequency characteristic under the ZVS condition was analyzed, indicating that achieving the high frequency requires small shunt capacitance. To validate the analysis, a class-D inverter was designed with minimum shunt capacitance, formed solely by the nonlinear parasitic capacitance. As a result, the class-D inverter successfully achieved ZVS operation at high frequencies, confirming the validity of the analytical model.

†The author is with Nagoya University, Nagoya-Shi, 464-8601 Japan.

In this paper, we further analyze the output power characteristics under the ZVS condition based on the analytical model presented in [32]. The expression of the output power is derived as a function of the output current angle phase, duty, DC input voltage, and load impedance. The characteristics of the function show that the high output power can be achieved under the ZVS condition with 0° output current phase (class-DE mode), large duty, and high DC input voltage when the load impedance is determined. Furthermore, we derive this paper's design equation for the external capacitor. The shunt capacitance can be designed through the design equation by combining the nonlinear parasitic capacitance with the linear external capacitors, allowing a wide range of frequency designs under the ZVS condition. To verify the usability of the design procedure for applying the class-D ZVS inverter to EV WPT systems, we set the design frequency to 85kHz. Additionally, to demonstrate the validity of the design procedure, we design two class-D inverters—one with Si-MOSFETs and the other with SiC-MOSFETs. In the design with Si-MOSFETs, we compare the design accuracy of ZVS operation and output power between the conventional and proposed models under the same design specification. The compared result reveals successful ZVS operation in the proposed model while failing in the conventional model. Moreover, the output power obtained by the proposed model is higher and closer to the analytical value than that obtained by the conventional model. To validate the analyzed output power characteristics, three additional design examples are presented. The result waveforms all satisfy the ZVS operation, and the measured output powers demonstrated the output power characteristics. Similar results are obtained in the SiC-MOSFET design, further confirming the validity of the design procedure and the output power characteristics. Furthermore, the condition for obtaining the maximum output power under the ZVS condition is analyzed. The analytical result indicates that the power MOSFETs with smaller parasitic capacitance can obtain higher maximum output power. To verify the analysis, the maximum output power under the ZVS condition obtained by using Si-MOSFETs and SiC-MOSFETs are compared. The simulated result shows that the SiC-MOSFET with smaller parasitic capacitance obtains a higher maximum output power than using Si-MOSFET.

2. Class-D Half-bridge ZVS Inverter with Linearized Parasitic Capacitance

2.1 Nonlinear Parasitic Capacitance Linearization

The nonlinear parasitic capacitance C_{ds} is typically expressed by (1) [14][31-37], where C_{j0} is the junction capacitance at v_{ds} = 0V, V_{bi} is the built-in potential voltage, and m is the grading coefficient. The typical value of V_{bi} can be calculated at about 0.6V for the Si device and 3V for the SiC device [38]. In real devices' modeling, it is fitted to other values [33], [36-37]. The grading coefficient m is irrelevant to the device's material but related to the gradient of the doping concentration for the drift layer [38-39]. In practical devices' modeling, m can be various values [35]. In [33-34], m is fixed at a typical value of 0.5. In [35-37], m is fitted by other values.

$$C_{ds}(v_{ds}) = \frac{C_{j0}}{(1+\frac{v_{ds}}{V_{bi}})^m} \tag{1}$$

The equation can be mathematically transformed into (2), where the $C_{DS(VDS)}$ at V_{DS} is a specification of the power device's datasheet.

$$C_{ds}(v_{ds}) = C_{DS(V_{DS})}\left(\frac{V_{DS}+V_{bi}}{v_{ds}+V_{bi}}\right)^m \tag{2}$$

According to [32], the nonlinear parasitic capacitance C_{ds} can be transformed to the charge-related equivalent linear capacitance C_{dseq} by (3).

$$\begin{aligned} C_{dseq}(v_{ds}) &= \frac{1}{v_{ds}}\int_{-V_{bi}}^{v_{ds}} C_{ds}(v_{ds})dv_{ds} \\ &= \frac{C_{DS(V_{DS})}(V_{DS}+V_{bi})^m}{v_{ds}}\frac{(v_{ds}+V_{bi})^{-m+1}}{-m+1} \end{aligned} \tag{3}$$

2.2 Equivalent Circuit

The equivalent circuit of the class-D half-bridge ZVS inverter containing the linearized parasitic is shown in Fig.1. The circuit consists of a DC voltage source V_I, two power devices M_1 and M_2, a series-resonant tank L_r-C_r, and a load resistance R. The power device contains a body-diode B and a linearized parasitic capacitance C_{dseq}. Besides, there is a linear external capacitor C_{ex} in parallel connection with the power device's drain and source. The linearized parasitic capacitance C_{dseq} and external capacitor C_{ex} constitute the shunt capacitance together as C_s. To conduct the ZVS operation, an extra inductor L_x is needed to realize the inductive load.

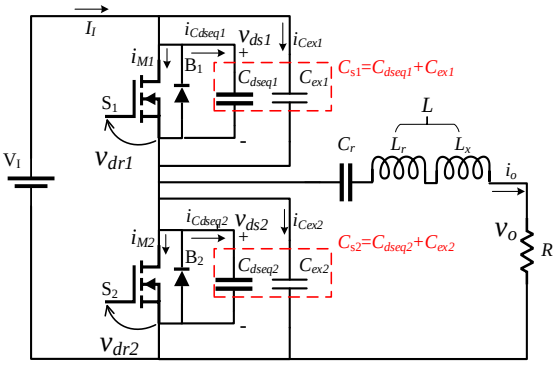


Fig. 1. Equivalent circuit for analysis

2.3 ZVS Operation

Fig. 2. shows the nominal waveforms of the class-D half-bridge inverter in ZVS operation. The $\omega = 2\pi f$ expresses the angular frequency and $\theta = \omega t$ expresses the angular time. The power device is regarded as ideal. The gate-driving

voltage v_{dr1} and v_{dr2} drive the power devices at duty ratio D and frequency f. The phase angle of the output current lags behind that of the output voltage by φ for the effect of the inductive load. As described in [32], during the deadtime t_d, both power devices are off. One of the shunt capacitances is charged by the output current and the other is discharged. When the low-side power device's voltage v_{ds2} falls to zero, the low-side power device's current i_{s2} starts to flow through the body-diode in the time interval from π to $\pi+\varphi$, during which the drain-source voltage keeps zero. If the rising edge of the gate-driving voltage v_{dr2} comes in the time interval from π to $\pi+\varphi$, the low-side switch is turned on at a zero drain-source voltage, conducting the ZVS operation.

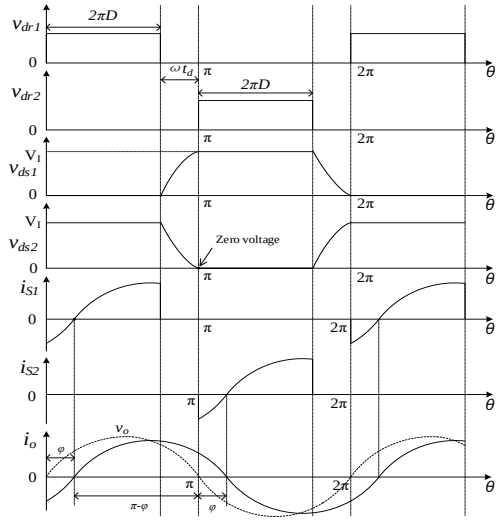


Fig. 2. Nominal waveforms of class-D half-bridge ZVS inverter

3. Circuit Modeling

3.1 Assumptions

Based on the equivalent circuit in Fig.1. and the ZVS operation waveform in Fig. 2. The circuit is mathematically modeled under the following assumptions:

1) The shunt capacitance is composed of the linearized parasitic capacitance and a linear external capacitor.

2) The power device is assumed ideal in this circuit, meaning zero-switching time, zero on-resistances, and infinite off-resistances.

3) The gate-driving voltages are ideal symmetric square waveforms, and their duty ratios range by $0 \le D \le 0.5$.

4) The definition formula of the loaded quality factor Q_L of the C_r-L-R series circuit is shown below,

$$Q_L = \frac{\omega L}{R} \tag{4}$$

Q_L is assumed sufficiently high, so that the output current can be regarded as an ideal sinusoidal wave as

$$i_o = \frac{V_m}{R}\sin(\omega t - \varphi) = I_m \sin(\omega t - \varphi) \tag{5}$$

where V_m and I_m are the amplitudes and the φ is the phase difference compared to the output voltage which is shown in Fig. 2.

5) The resonant filter L_r-C_r is assumed ideal and only the fundamental frequency component remains from the filter. The resonant inductance L is divided into L_r and L_x virtually, namely,

$$L = L_r + L_x \tag{6}$$

Thereby, the resonant frequency f is determined by $f = 1/2\pi\sqrt{L_r C_r}$. Additionally, L_x yields a phase shift of the output current.

6) All the components have no parasitic components.

7) All the components on the high-side and low-side are identical. Hence, as shown in Fig. 1. the total sum of the shunt capacitance of both sides can be defined as

$$\begin{aligned} C_{st} &= C_{s1} + C_{s2} \\ &= (C_{dseq1} + C_{ex1}) + (C_{dseq2} + C_{ex2}) \\ &= 2(C_{dseq} + C_{ex}) = 2C_s \end{aligned} \tag{7}$$

8) The switches' voltages satisfy the ZVS operation results which are

$$v_{ds1}(2\pi) = 0 \quad \textit{and} \quad v_{ds2}(2\pi) = V_I \tag{8}$$

$$v_{ds1}(\pi) = V_I \quad \textit{and} \quad v_{ds2}(\pi) = 0 \tag{9}$$

3.2 Output Voltage Relation via ZVS Condition

In [32], the relationship among output voltage amplitude V_m, angle frequency ω, total sum of shunt capacitance C_{st}, duty ratio D, DC input voltage V_I, and output current phase angle φ under the ZVS condition has been derived as (10).

$$V_m = \frac{\omega C_{st} R}{2\cos(\pi D - \varphi)\cos\pi D} V_I \tag{10}$$

To conduct the ZVS operation, the derivative of v_{ds2} should be minus or zero [25]. When the derivative is just equal to zero at $\theta = \pi$, not only the ZVS condition but also the class-DE zero-derivative-switching (ZDS) condition is satisfied. The derivative has been obtained in [32] as

$$\alpha = -\frac{\sin\varphi}{2\cos(\pi D - \varphi)\cos\pi D} V_I \tag{11}$$

As discussed above, the derivative α should be

$$\alpha \le 0 \tag{12}$$

As the DC input voltage V_I is not zero, it can be inferred that the only condition to obtain the result of $\alpha = 0$ is

$$\varphi = 0^\circ \tag{13}$$

Hence, (13) is the condition of the class-DE mode.

3.3 Output Voltage Relation via Fourier Expansion

It has been indicated in [32] that the voltage across the phase shift inductor L_x and the load resistance R just constitute the fundamental-frequency component of the low-side switch voltage $v_{ds2}(\theta)$ for $0 \le \theta \le 2\pi$, where the voltage across L_x is the cosine function part and the voltage across R is the sine function part. The expressions of the output voltage amplitude V_m and the phase shift inductor voltage amplitude V_{Lx} have been derived as (14) and (15).

$$V_m = 2V_I \cos\varphi\{\pi + \frac{1}{\omega C_{st} R}[\frac{1}{2}\cos 2\varphi + \frac{1}{2}\cos(4\pi D - 2\varphi) + \cos(2\pi D - 2\varphi) + \cos 2\pi D + 1]\}^{-1} \tag{14}$$

$$V_{Lx} = \omega L_x I_m = \frac{V_I}{\pi}\{2\sin\varphi + [\pi - 2\pi D - \frac{1}{2}\sin(4\pi D - 2\varphi) + \sin(2\pi D - 2\varphi) - \sin 2\pi D][2\cos\pi D\cos(\pi D - \varphi)]^{-1}\} \tag{15}$$

3.4 Frequency and Shunt Capacitance Relation

By combining (14) with (10), a new equation is obtained as (16), within the angle frequency ω, the total sum of shunt capacitance C_{st}, duty ratio D, output current phase angle φ, and load impedance R. The obtained (16) also satisfies the ZVS condition from (10).

$$\omega C_{st} R = \frac{\sin(2\pi D - 2\varphi)\sin 2\pi D}{\pi} \tag{16}$$

It can be inferred that $\omega C_{st}R$ can be a function of output current phase angle φ and duty ratio D under the ZVS condition. By the function, the necessary total sum of shunt capacitance C_{st} can be solved when the angle frequency ω, output current φ, duty ratios D, and load impedance R are determined. For the range of φ, according to α in (12), and $\omega C_{st}R$ in (16), with the condition $\alpha \le 0$, and $\omega C_{st}R \ge 0$, the range of φ can be limited to

$$0 \le \varphi \le \pi D \tag{17}$$

4. Power Relation

Considering relations among the amplitude of the output voltage V_m, the input voltage V_I, and the load impedance R, the output power P_o under the ZVS condition can be expressed by the corresponding circuit parameters. From (10) and (16), the analytical output power can be expressed as

$$P_o = \frac{V_m^2}{2R} = \frac{2V_I^2 \sin^2(\pi D - \varphi)\sin^2 \pi D}{\pi^2 R} \tag{18}$$

The derived equation of the output power results in a function of the DC input voltage V_I, load impedance R, output current phase angle φ, and duty ratio D. It is obvious that the output power is positively correlated with V_I and inversely proportional to R. At steady state operation, the DC input voltage V_I and load impedance R are constant, so the output power can be normalized as a function of the output current phase angle φ when duty ratio D is regarded as a variable constant, which is

$$\frac{P_o R}{V_I^2} = \frac{2\sin^2(\pi D - \varphi)\sin^2 \pi D}{\pi^2} \tag{19}$$

To figure out the characteristics of the obtained normalized output power, the function is plotted in Fig. 3. It shows that the normalized output power can always reach its maximum value at any duty ratio when $\varphi = 0^\circ$. Thus, $\varphi = 0^\circ$ becomes the condition for achieving maximum output power at any duty ratio.

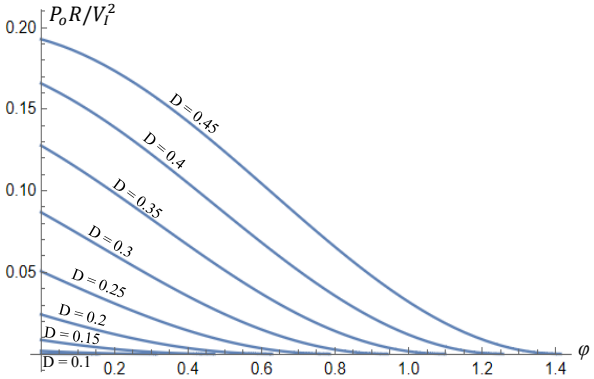


Fig. 3. Plotted normalized output power versus φ

Substituting $\varphi = 0^\circ$ to (19), the normalized output power can be obtained as

$$\frac{P_o R}{V_I^2} = \frac{2\sin^4 \pi D}{\pi^2} \tag{20}$$

The normalized maximum output power is plotted in Fig. 4. For $0 \le D \le 0.5$ (Assumption 3), the normalized output power results in a monotone increasing function of the duty ratio D. Thus, it can be inferred that to obtain high output power, the duty ratio should be large under the condition of $\varphi = 0^\circ$.

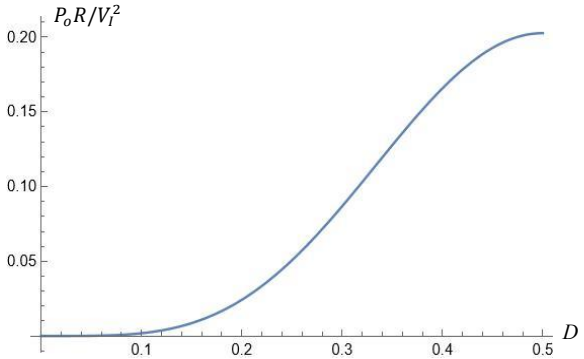


Fig. 4. Plotted normalized output power versus duty ratio D

From the analyzed results above, it can be inferred that the optimal condition to achieve high output power with a fixed load impedance under the ZVS condition is that 0° output current phase angle, large duty ratio, and high DC input voltage. The characteristics are summarized in Table 1.

Table 1. Characteristics of the output power under the ZVS condition

	Fixed variable		Result
Property 1	φ ($\varphi \geq 0^\circ$)	D ($0 \geq D \geq 0.5$)	P_o & V_I Positive Correlation
Property 2	V_I	D ($0 \geq D \geq 0.5$)	P_o & φ ($\varphi \geq 0^\circ$) Negative Correlation
Property 3	V_I	φ ($\varphi \geq 0^\circ$)	P_o & D ($0 \geq D \geq 0.5$) Positive Correlation

5. Design Equation

The design equations of the circuit components, such as resonant capacitor C_r, resonant inductor L_r, phase shift inductor L_x, and linear external capacitor C_{ex}, in the class-D half-bridge ZVS inverter are obtained as below:

From (15), L_x can be solved as

$$L_x = \frac{1}{\pi\omega^2 C_{st}}[\pi - 2\pi D + 4\sin\varphi\cos\pi D\cos(\pi D - \varphi) - \frac{1}{2}\sin\varphi + \frac{1}{2}\sin(4\pi D - 2\varphi) + \sin(2\pi D - 2\varphi) - \sin 2\pi D] \quad (21)$$

Therefore, from (4) and (6), we have

$$L_r = L - L_x = \frac{Q_L R}{\omega} - L_x \quad (22)$$

Therefore, from assumption 7), C_r can be solved as

$$C_r = \frac{1}{(2\pi f)^2 L_r} \quad (23)$$

From Assumption 7) and (7), it can be inferred that the shunt capacitance of each side $C_{s1,2}$ is just half of the total sum shunt capacitance C_{st}. Thus, the equation to obtain the necessary linear external capacitor can be expressed as

$$C_{ex} = C_s - C_{dseq} = \frac{C_{st}}{2} - C_{dseq} \quad (24)$$

6. Design of 85kHz Class-D Half-bridge ZVS Inverter with a 650V/30A Si-MOSFET

6.1 C_{ds} Linearization of a 650V/30A Si-MOSFET

The Si-MOSFET is chosen to R6530ENZ4 (650V/30A) [40]. According to (2), the C_{ds} can be modeled if the coefficients of m, V_{bi} ,$V_{DS,}$ and $C_{DS(VDS)}$ are determined properly. There are two steps to determine the coefficients. First, figuring out the analytical or typical values of the parameters. Second, utilizing the mathematical tool to optimize the values. For the first step, the V_{DS}, $C_{DS(VDS)}$ can be obtained from [40] by V_{DS} = 25V, $C_{DS(VDS)}$ = 2070pF. According to the defining formula of V_{bi} in [14][38], the analytical value of V_{bi} for Si device can be calculated by V_{bi} = 0.57V. The grad coefficient m is typically determined to be 0.5. In Fig.5, the C_{ds} model with the analytical coefficients is plotted into curve. It can be seen that there is an offset from the data points extracted from the datasheet [40]. To eliminate the offset, we need to utilize the mathematical tool to optimize the values and fit the curve, which is the second step. We keep V_{DS} = 25V as analyzed and set m to a variable. Then we adjust V_{bi} and $C_{DS(VDS)}$ manually bit by bit and utilize the tool to optimize the m simultaneously. After repeated adjustments and fittings, the optimal values are obtained. The analytical and fitted coefficients are listed in Table 2. Fig.5 shows that the curve with fitted coefficients matches better with the datasheet. The method of coefficient fitting for C_{ds} modeling has been utilized regularly [36-37].

Table 2. C_{ds} model coefficients of the Si-MOSFET

Parameter	Analytical	Fitted
V_{bi} (V)	0.57	0.7
m	0.5	0.8
$C_{DS(VDS)}$ (pF)	2070	800
V_{DS} (V)	25	25

With the fitted coefficients, the nonlinear parasitic capacitance C_{ds} of the Si-MOSFET can be modeled by

$$C_{ds-Si}(v_{ds}) = 800 \times \left(\frac{25+0.7}{v_{ds}+0.7}\right)^{0.8} \text{(pF)} \quad (25)$$

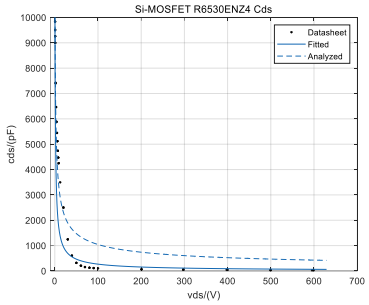


Fig. 5. Plotted C_{ds} of the Si-MOSFET

From (3), the linearized parasitic capacitance $C_{dseq\text{-}Si}$ of the Si-MOSFET can be modeled by (26), and the graph of the modeled $C_{dseq\text{-}Si}$ is plotted in Fig. 6.

$$C_{dseq-Si}(v_{ds}) = \frac{800 \times 25.7^{0.8}}{0.2 v_{ds}}(v_{ds}+0.7)^{0.2} \text{(pF)} \quad (26)$$

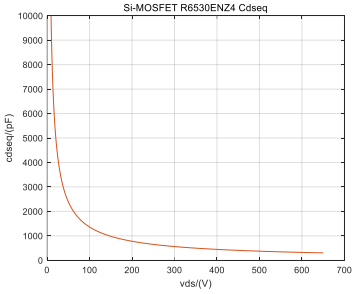


Fig. 6. Plotted C_{dseq} of the Si-MOSFET

6.2 Comparison with the Conventional Model

This section is to compare the design accuracy for ZVS operation and output power between the proposed model and the conventional model [25]. The common design specification for the class-D half-bridge ZVS inverter is given by: operating frequency f = 85kHz, load resistance R = 50Ω, and loaded quality factor Q_L = 5 (which is sufficiently high [14]). To obtain high output power, the output current phase angle φ is given by $\varphi = 0^{\circ}$, (means class-DE mode from (13)). The duty ratio and DC input voltage are given by large values which are: D = 0.45, V_I = 300V. The design procedure is given below:

6.2.1 Shunt Capacitance Design by Conventional Model.

As the nonlinear parasitic capacitance is neglected in the conventional model, the necessary shunt capacitance is only formed by the linear external capacitor. For $\varphi = 0^{\circ}, D = 0.45$, the value of $\omega C_{st}R$ can be calculated from (16) that

$$\omega C_{st} R = 0.0304 \tag{27}$$

As the frequency f = 85kHz, R = 50Ω, the total sum of the shunt capacitance can be obtained as

$$C_{st} = \frac{0.0304}{\omega R} = \frac{0.0304}{2\pi fR} = 1.138nF \tag{28}$$

The shunt capacitance paralleled with the MOSFET on each side can be calculated as

$$C_{ex(con)} = \frac{1}{2} C_{st} = 0.569nF \tag{29}$$

6.2.2 Shunt Capacitance Design by the Proposed Model.

With the proposed model, the shunt capacitance can be designed with the combination of nonlinear parasitic capacitance and a linear external capacitor. From (26), as V_I = 300V, the linearized capacitance $C_{dseq\text{-}Si}$ of the Si-MOSFET can be calculated as

$$C_{dseq-Si(300V)} \approx 0.560nF \tag{30}$$

From (24), the necessary linear external capacitor is

$$C_{ex} == \frac{C_{st}}{2} - C_{dseq-Si(300V)} = 0.009nF \tag{31}$$

6.2.3 Resonant Components Design

The design procedure of the resonant components is common between this paper and [25].

Substituting the determined values that ω (for f = 85kHz), C_{st} (from (28)), φ = 0◦, D = 0.45, to (21), the phase shift inductance can be calculated as

$$L_x \approx 19.874uH \tag{32}$$

As the frequency and loaded quality factor are determined by f = 85kHz, Q_L = 5, the total inductance can be calculated as

$$L = \frac{Q_L R}{2\pi f} \approx 468.103uH \tag{33}$$

Thus, the value of the resonant inductor can be obtained as

$$L_r = L - L_x = 448.229uH \tag{34}$$

The resonant capacitor can be calculated as

$$C_r = \frac{1}{(2\pi f)^2 L_r} \approx 7.822nF \tag{35}$$

6.2.4 ZVS Operation Comparison

To avoid the influence of parasitic components on the comparison results, the comparison is conducted by simulation. The simulation schematic with the Si-MOSFET SPICE model is shown in Fig. 7. The gate-driving voltage is chosen to a proper voltage of 16V [40]. An equivalent series resistance (ESR) r_{ESR} is set in the C_r-L-R series circuit. The equivalent series inductances (ESL) are also set into the wire. The values of both ESR and ESL are set to zero. Other designed parameters are listed in Table 3.

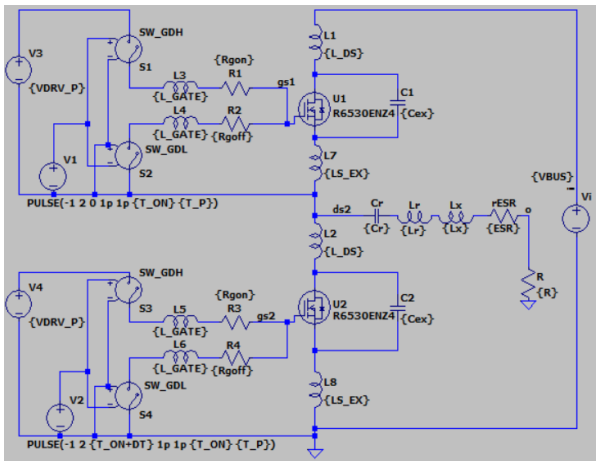


Fig. 7. Simulation schematic

Table 3. Simulation parameters for model comparison

Parameter	Symbol	Conventional	Proposed
Phase angle	φ	0°	0°
Duty	D	0.45	0.45
Input voltage	V_I	300V	300V
Load resistance	R	50Ω	50Ω
External capacitor	C_{ex}	0.569nF	0.009nF
Parasitic capacitance	C_{ds}	0nF (Neglected)	0.560nF (Linearized)
Loaded quality factor	Q_L	5	5
Total inductor	L_r+L_x	468.103uH	468.103uH
Resonant capacitor	C_r	7.822nF	7.822nF
ESR	r_{ESR}	0Ω	0Ω
ESL	L_1~L_8	0H	0H

The simulated waveforms are shown in Fig. 8. In the waveform of the proposed model, the turn-on edge of $v_{(gs2)}$ comes just directly after the $v_{(ds2)}$ (proposed) decreases to zero, meaning that the ZVS operation is successfully conducted. However, in the waveform of the conventional model, the $v_{(ds2)}$ (conventional) is still about 60V when the turn-on edge has come, meaning that the ZVS operation failed. The compared result shows that the design accuracy for ZVS operation by the proposed model is higher than that by the conventional model.

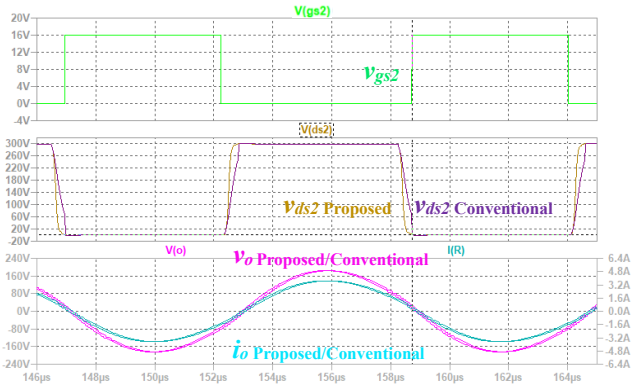


Fig. 8. Simulated waveform by conventional and proposed model

6.2.5 Output Power Comparison

The analytical output power equation is common between this paper and [25]. From (20), in condition of $\varphi = 0^\circ$, $D = 0.45$, $V_I = 300$V, $R = 50\Omega$, the analytical output power can be calculated as

$$P_o = \frac{2V_I^2 \sin^4 \pi D}{\pi^2 R} \approx 347.12W \tag{36}$$

Table 4. indicates that the simulated output power by the proposed model is higher than that of the conventional model and is closer to the analyzed value. This discrepancy arises because the ZVS operation failed in the design using the conventional model, resulting in more energy dissipation by hard switching. The comparison demonstrates that the proposed model achieves higher design accuracy for output power than that of the conventional model.

Table 4. Simulated output powers comparison

Analytical	Simulated	
	Conventional	Proposed
347.12W	344.59W	346.09W

6.3 Output Power Characteristics Verification

The common design specification of the 85kHz class-D ZVS inverter is given by: operating frequency $f = 85$kHz, load resistance $R = 50\Omega$, and the loaded quality factor $Q_L = 5$. To verify the validity of the output power characteristics, other specifications of duty ratio, DC input voltage, and output current phase angle are given in four conditions:

Condition 1, $D = 0.45$, $V_I = 300$V, $\varphi = 0^\circ$.
Condition 2, $D = 0.4$, $V_I = 300$V, $\varphi = 0^\circ$.
Condition 3, $D = 0.4$, $V_I = 200$V, $\varphi = 0^\circ$.
Condition 4, $D = 0.45$, $V_I = 300$V, $\varphi = 1.8^\circ$.

Compared to condition 2, condition 3 is given to verify the relation between the DC input voltage V_I and output power P_o (Property 1 in Table 1).

Compared to condition 1, condition 4 is given to verify the relation between output current phase angle φ and output power P_o. (Property 2 in Table 1).

Compared to condition 1, condition 2 is given to verify the relation between duty D and output power P_o (Property 3 in Table 1).

As for the experiment, Fig. 9. shows the self-made prototype of the class-D half-bridge ZVS inverter. The Si-MOSFETs are assembled on the printed circuit board (PCB). The Si-MOSFET's drain and source are paralleled with an external capacitor to form the shunt capacitance with the internal nonlinear parasitic capacitance. The gate of the SiC-MOSFET is driven by the gate driver with a voltage of 16V which is identical to the simulation. The gate-driving signal is provided at 85kHz by a low-noise function generator. The resonant inductor is selected to an inductor which is made by a Fe-Ni toroidal core with 2mm enameled copper wire, providing an 11A rated current. The external capacitors and resonant capacitors are utilized by the 2kV multilayer ceramic capacitors (MLCC). The load is utilized by a 50Ω dummy load which is integrated in a power meter. The power meter is connected to the AC output coaxial port through a 50dB attenuator. The duty ratio of the gate-driving signal is adjustable through an RC integral circuit with variable resistance. To compare the measured results with those of analytical and simulated under identical conditions, the measured value of ESR is set identically in the simulation circuit and output power analytical equation. The specification and design parameters for analytical, simulation, and experiment are all listed in Table 5. The experimental waveforms are shown from Fig. 10. to Fig. 13.

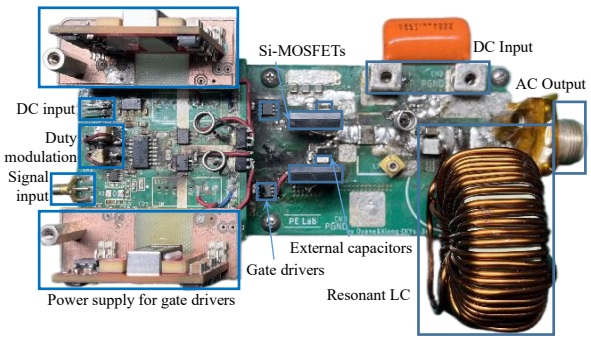


Fig. 9. Prototype for experimental verification

Table 5. Specifications and parameters of the designed Class-D half-bridge ZVS inverter with Si-MOSFET

	Condition 1			Condition 2			Condition 3			Condition 4		
Parameter	Analytical	Simulated	Measured	Analytical	Simulated	Measured	Analytical	Simulated	Measured	Analytical	Simulated	Measured
v_{dr}**(V)**	—	16.0V	16.09V	—	16.0V	16.09V	—	16.0V	16.12V	—	16.0V	15.94V
D	0.45	0.45	0.45	0.4	0.4	0.4	0.4	0.4	0.4	0.45	0.45	0.45
φ **( )**	0°	0°	0.18°	0°	0°	0.18°	0°	0°	0.32°	1.8°	1.8°	2.04°
R**(Ω)**	50Ω	50Ω	50.18Ω	50Ω	50Ω	50.18Ω	50Ω	50Ω	50.18Ω	50Ω	50Ω	50.18Ω
V_I**(V)**	300V	300V	300V	300V	300V	300V	200V	200V	200V	300V	300V	300V
C_{ex}**(nF)**	0.009nF	0.009nF	0.010nF	1.499nF	1.499nF	1.494nF	1.285nF	1.285nF	1.279nF	0.113nF	0.113nF	0.110nF
L**(uH)**	468.10uH	468.10uH	468.90uH	468.10uH	468.10uH	468.90uH	468.10uH	468.10uH	468.90uH	468.10uH	468.10uH	468.90uH
C_r**(nF)**	7.822nF	7.822nF	7.819nF	8.216nF	8.216nF	8.220nF	8.216nF	8.216nF	8.219nF	8.091nF	8.091nF	8.082nF
Q_L	5	5	4.99	5	5	4.99	5	5	4.99	5	5	4.99
r_{ESR}**(Ω)**	3.41Ω	3.41Ω	3.41Ω	3.38Ω	3.38Ω	3.38Ω	3.41Ω	3.41Ω	3.41Ω	3.42Ω	3.42Ω	3.42Ω
P_o**(W)**	304.21W	305.22W	311.43W	262.09W	267.18W	268.32W	116.23 W	118.64 W	122.56 W	300.78 W	284.08W	286.54 W
T_c**(°C)**	—	25°C	31.4°C	—	25°C	31.1°C	—	25°C	28.2°C	—	25°C	29.8°C

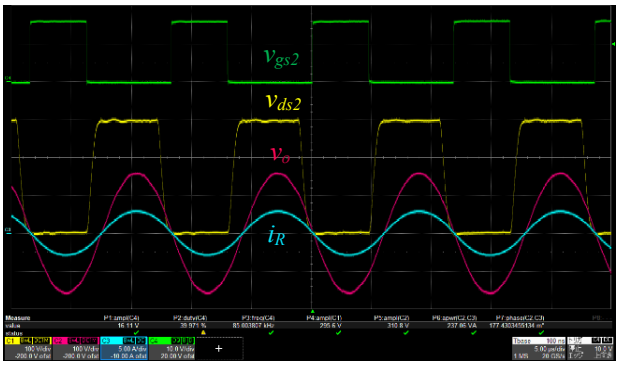


Fig. 10. Experimental waveform by Si-MOSFET in condition 1

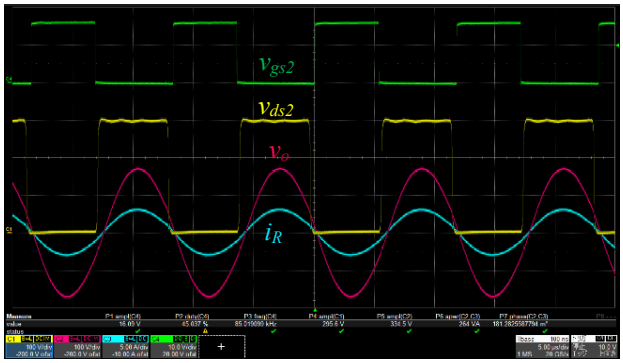


Fig. 11. Experimental waveform by Si-MOSFET in condition 2

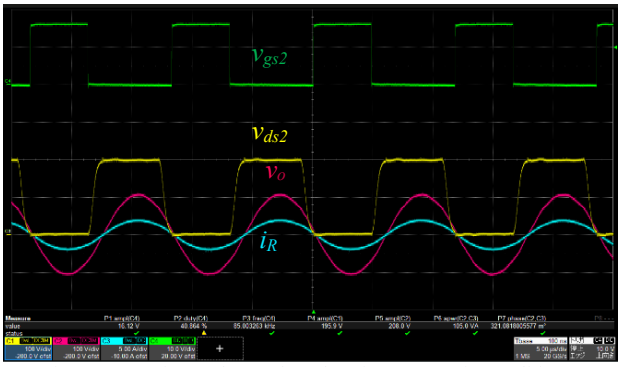


Fig. 12. Experimental waveform by Si-MOSFET in condition 3

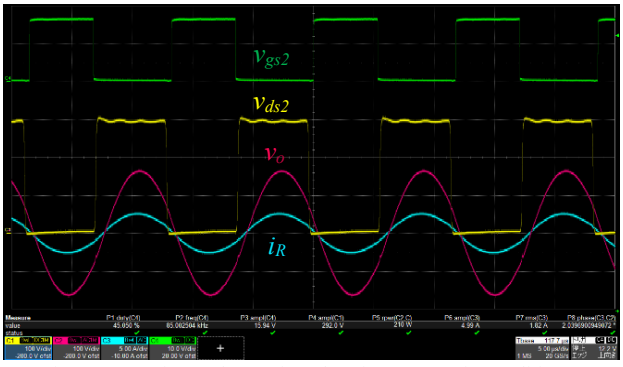


Fig. 13. Experimental waveform by Si-MOSFET in condition 4

6.4 Result Analysis

Regarding the experimental waveforms, the ZVS operations are successfully conducted in all conditions. The measured output powers align closely with simulated and analytical results with limited error. In the practical circuit, the high harmonics cannot be completely filtered by the non-ideal resonator. The harmonics are also identified by the power meter, resulting in the measured result being a little higher than the analytical in Conditions 1,2 and 3. On the other hand, when the output current phase angle φ is not designed at 0° in Condition 4, the extra inductance L_x for phase shift is not small anymore, making the practical load impedance a little larger than 50Ω. This is the reason that the measured result is lower than the analytical in Condition 4.

Table 6. summarizes the characteristics of the measured output powers. Comparing the output powers between conditions 2 and 3, it reveals that a higher DC input voltage results in higher output power verifying Property 1 in Table 1. Similarly, comparing the output powers between conditions 1 and 4, it reveals that 0° output current phase angle (class-DE mode) results in higher output power than that of 1.8° (not class-DE mode), verifying Property 2 in Table 1. Comparing the output powers between conditions 1 and 2, it reveals that a larger duty results in higher output power, verifying Property 3 in Table 1. Finally, the maximum output power resulted in condition 1 with class-DE mode, largest duty, and highest DC input voltage, verifying the output power characteristics in general.

Table 6. Verified output power property by Si-MOSFET

Condition 2 vs. Condition 3			Result
$V_{I2} > V_{I3}$	$0° = \varphi_2 = \varphi_3$	$D_2 = D_3$	$P_{o2} > P_{o3}$
Condition 1 vs. Condition 4			Result
$V_{I1} = V_{I4}$	$0° = \varphi_1 < \varphi_4$	$D_1 = D_4$	$P_{o1} > P_{o4}$
Condition 1 vs. Condition 2			Result
$V_{I1} = V_{I2}$	$0° = \varphi_1 = \varphi_2$	$D_1 > D_2$	$P_{o1} > P_{o2}$

7. Design of 85kHz Class-D Half-bridge ZVS Inverter with a 650V/30A SiC-MOSFET

7.1 C_{ds} Linearization of a 650V/30A SiC-MOSFET

The SiC-MOSFET is chosen to SCT3080AL (650V/30A) [41]. The analytical and fitted coefficients of V_{DS}, $C_{DS(VDS)}$, V_{bi}, and m are listed in Table 7. The plotted graph of the C_{ds} with analytical and fitted coefficients is shown in Fig. 14. Compared to the graph with analytical coefficients, the graph with fitted coefficients matched a lot to the data points extracted from the datasheet [41].

Table 7. C_{ds} model coefficients of the SiC-MOSFET

Parameter	Analytical	Fitted
V_{bi} (V)	2.996	2
m	0.5	0.5
$C_{DS(VDS)}$ (pF)	20	32
V_{DS} (V)	500	500

With the fitted coefficients, the nonlinear parasitic capacitance C_{ds} of the SiC-MOSFET can be modeled by

$$C_{ds-SiC}(v_{ds}) = 32\times\left(\frac{500+2}{v_{ds}+2}\right)^{0.5} \text{ (pF)} \qquad (37)$$

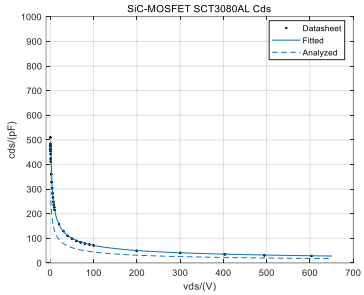


Fig. 14. Plotted C_{ds} of the SiC-MOSFET

From (3), the linearized parasitic capacitance $C_{dseq\text{-}SiC}$ of the SiC-MOSFET can be modeled by (38), and the function of the linearized parasitic capacitance $C_{dseq\text{-}SiC}$ is plotted in Fig. 15.

$$C_{dseq-SiC}(v_{ds}) = \frac{32\times 502^{0.5}}{0.5v_{ds}}(v_{ds}+2)^{0.5} \text{ (pF)} \qquad (38)$$

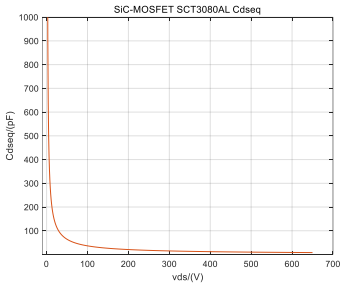


Fig. 15. Plotted C_{dseq} of the SiC-MOSFET

7.2 Output Power Characteristics Verification

Similar to the verification of the class-D ZVS inverter with the Si-MOSFETs, the design specifications are given in four conditions:

Condition 1, $D = 0.45$, $V_I = 300$V, $\varphi = 0^\circ$.
Condition 2, $D = 0.4$, $V_I = 300$V, $\varphi = 0^\circ$.
Condition 3, $D = 0.4$, $V_I = 200$V, $\varphi = 0^\circ$.
Condition 4, $D = 0.45$, $V_I = 300$V, $\varphi = 1.8^\circ$.

The design specifications and parameters are listed in Table 8. The experimental waveforms are shown from Fig.16 to Fig.19.

Table 8. Specifications and parameters of the designed Class-D half-bridge ZVS inverter with SiC-MOSFET

	Condition 1			Condition 2			Condition 3			Condition 4		
Parameter	Analyzed	Simulated	Measured	Analyzed	Simulated	Measured	Analyzed	Simulated	Measured	Analyzed	Simulated	Measured
v_{dr}**(V)**	—	16.3V	16.27V	—	16.3V	16.26V	—	16.3V	16.27V	—	16.3V	16.27V
D	0.45	0.45	0.45	0.4	0.4	0.4	0.4	0.4	0.4	0.45	0.45	0.45
φ **(°)**	0°	0°	0.18°	0°	0°	0.27°	0°	0°	0.23°	1.8°	1.8°	1.76°
R**(Ω)**	50Ω	50Ω	50.18Ω	50Ω	50Ω	50.18Ω	50Ω	50Ω	50.18Ω	50Ω	50Ω	50.18Ω
V_I**(V)**	300V	300V	300V	300V	300V	300V	200V	200V	200V	300V	300V	300V
C_{ex}**(nF)**	0.486nF	0.486nF	0.485nF	1.976nF	1.976nF	1.980nF	1.958nF	1.958nF	1.961nF	0.591nF	0.591nF	0.589nF
L**(uH)**	468.10uH	468.10uH	468.90uH	468.10uH	468.10uH	468.90uH	468.10uH	468.10uH	468.90uH	468.10uH	468.10uH	468.90uH
C_r**(nF)**	7.822nF	7.822nF	7.819nF	8.216nF	8.216nF	8.232nF	8.216nF	8.216nF	8.198nF	8.091nF	8.091nF	8.073nF
Q_L	5	5	4.99	5	5	4.99	5	5	4.99	5	5	4.99
r_{ESR}**(Ω)**	3.39Ω	3.39Ω	3.39Ω	3.41Ω	3.41Ω	3.41Ω	3.41Ω	3.41Ω	3.41Ω	3.40Ω	3.40Ω	3.40Ω
P_o**(W)**	304.44W	304.57W	306.53W	261.53W	265.17W	265.32W	116.23W	117.84 W	121.73 W	301.01W	283.95W	287.25 W
T_c**(°C)**	—	25°C	30.4°C	—	25°C	30.1°C	—	25°C	27.2°C	—	25°C	29.3°C

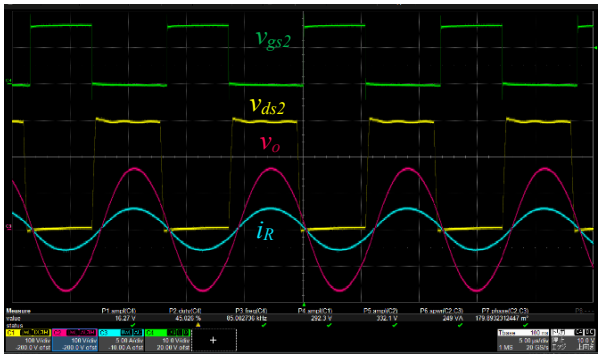


Fig. 16. Experimental waveform by SiC-MOSFET in condition 1

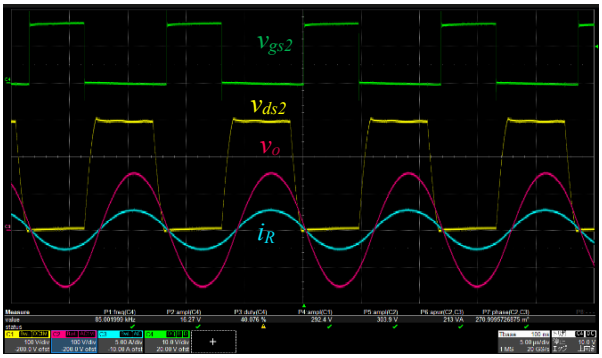


Fig. 17. Experimental waveform by SiC-MOSFET in condition 2

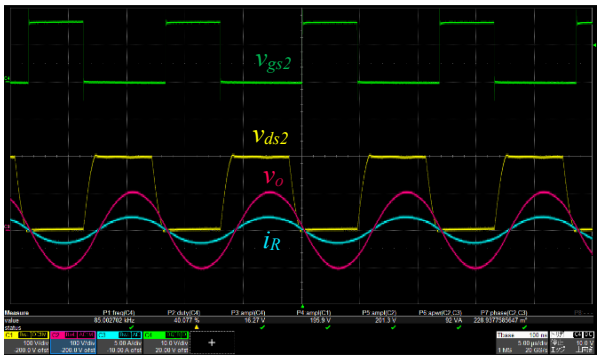


Fig. 18. Experimental waveform by SiC-MOSFET in condition 3

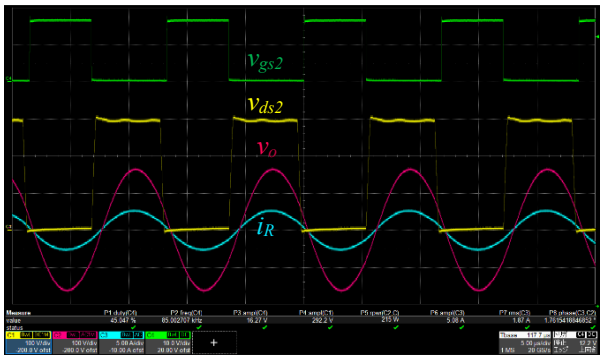


Fig. 19. Experimental waveform by SiC-MOSFET in condition 4

7.3 Result Analysis

Consistent with the Si-MOSFET, the experimental waveforms obtained by the SiC-MOSFET successfully demonstrate the ZVS operation in all conditions. The summarized output power properties in Table 9. also validate the characteristics in Table 1. The maximum output power obtained by the SiC-MOSFET resulted in Condition 1 with class-DE mode, largest duty, and highest DC input voltage.

Table 9. Verified output power property by SiC-MOSFET

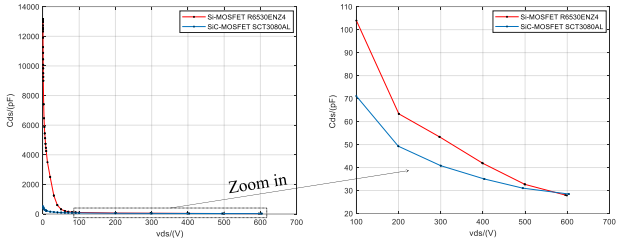
Condition 2 vs. Condition 3			Result
$V_{I2} > V_{I3}$	$0^\circ = \varphi_2 = \varphi_3$	$D_2 = D_3$	$P_{o2} > P_{o3}$
Condition 1 vs. Condition 4			Result
$V_{I1} = V_{I4}$	$0^\circ = \varphi_1 < \varphi_4$	$D_1 = D_4$	$P_{o1} > P_{o4}$
Condition 1 vs. Condition 2			Result
$V_{I1} = V_{I2}$	$0^\circ = \varphi_1 = \varphi_2$	$D_1 > D_2$	$P_{o1} > P_{o2}$

8. Comparison of Maximum Output Power between Si-MOSFET and SiC-MOSFET

In Chapters 6 and 7, the validity of the model for designing the class-D ZVS inverter has been verified by both Si-MOSFETs and SiC-MOSFETs. As the frequency of 85kHz is suitable for both types of MOSFETs, the ZVS operation performances are identical. However, as shown in Fig. 20, the nonlinear parasitic capacitance C_{ds} of the Si-MOSFET is much larger than that of the SiC-MOSFETs, especially in low v_{ds} area. For ZVS operation, a larger capacitance means a longer dead time for charge and discharge, so the duty becomes smaller, resulting in lower output power.

8.1 Analysis of Maximum Output Power under the ZVS condition

In Chapters 4 and 7, it has been verified that the condition for achieving high output power is high DC input voltage, 0° output current phase angle, and large duty. According to (20), with determined DC input voltage and 0° output current phase angle, the output power becomes an increasing function of the duty, indicating that the maximum output power is determined by the largest duty. (16) illustrates the relationship between duty and other parameters under the ZVS condition. By deriving this equation, it is possible to figure out the condition for obtaining the largest duty cycle under the ZVS condition. To achieve the maximum output



(a) (b)

Fig. 20 Comparison of the parasitic capacitance C_{ds} between Si-MOSFET and SiC-MOSFET
(a) Full scale (b) Zoom in

power, first of all, the output current phase angle should be determined by $\varphi = 0^\circ$, thus (16) can be transformed to

$$\omega C_{st} R = \frac{\sin^2 2\pi D}{\pi} \tag{39}$$

As the frequency and load impedance are usually determined by the design specification, they can be considered as constant. For the duty is defined as $0 \le D \le 0.5$, (39) can be transformed to

$$2\pi D = \sin^{-1}\sqrt{\pi\omega C_{st} R} \text{ ,where } 0 \le D \le 0.25 \tag{40}$$

$$2\pi D = \pi - \sin^{-1}\sqrt{\pi\omega C_{st} R} \text{ ,where } 0.25 < D \le 0.5 \tag{41}$$

To obtain the duty as large as possible, (41) is chosen as the significant solution. From (41), it can be inferred that the duty ratio D is a decreasing function of the total sum of the shunt capacitance C_{st}. Thus, the largest duty D_{max} can be obtained by the smallest shunt capacitance total sum $C_{stmin,}$ which is,

$$D_{\max} = \frac{\pi - \sin^{-1}\sqrt{\pi\omega C_{st\min} R}}{2\pi} \text{ , where } 0.25 < D \le 0.5 \tag{42}$$

From (7), it can be inferred that

$$C_{st\min} = 2(C_{dseq} + C_{ex})_{\min} \tag{43}$$

When the external capacitor is removed, the C_{ex} can be minimum as zero, thus,

$$C_{st\min} = 2C_{dseq\min} \tag{44}$$

Thus, (42) can transformed to

$$D_{\max} = \frac{\pi - \sin^{-1}\sqrt{2\pi\omega C_{dseq\min} R}}{2\pi}, \text{ where } 0.25 < D \le 0.5 \tag{45}$$

(45) means that the maximum duty is determined by the minimum of the linearized parasitic capacitance of the power MOSFET.

8.2 Maximum Duty Calculation for Si-MOSFET

From (26) and Fig. 6, it can be inferred that the linearized parasitic capacitance of Si-MOSFET $C_{dseq\text{-}Si}$ is a decreasing function of the drain-source voltage v_{ds}. To obtain the minimum of linearized parasitic capacitance, the DC input voltage should be set to maximum. The breakdown voltage of the Si-MOSFET is 650V [40]. Considering a margin of 1.5 times the input voltage for the voltage surge, the maximum DC input voltage is supposed to be 400V.

Substituting v_{dsmax} = 400V into (26), the minimum linearized parasitic capacitance of the Si-MOSFET can be obtained as

$$C_{dseq\min-Si} = 455(\text{pF}) \tag{46}$$

Substituting (46) to (45), the maximum duty of the Si-MOSFET can be obtained as

$$D_{\max-Si} = 0.4555 \tag{47}$$

8.3 Maximum Duty Calculation for SiC-MOSFET

From (38) and Fig. 15, it can be inferred that the linearized parasitic capacitance of SiC-MOSFET $C_{dseq\text{-}SiC}$ is a decreasing function of the drain-source voltage v_{ds}. To obtain the minimum of linearized parasitic capacitance, the DC input voltage should be set to maximum. As the breakdown voltage of the SiC-MOSFET is also 650V [41]., the maximum DC input voltage is supposed to be 400V.

Substituting v_{dsmax} = 400V into (38), the minimum linearized parasitic capacitance of the Si-MOSFET can be obtained as

$$C_{dseq\min-SiC} = 72(\text{pF}) \tag{48}$$

Substituting (48) to (45), the maximum duty of the Si-MOSFET can be obtained as

$$D_{\max-SiC} = 0.4825 \tag{49}$$

8.4 Maximum Output Power Comparison between Si-MOSFET and SiC-MOSFET under ZVS condition

As shown in Table 10, to verify the maximum output power, the parameters are designed with the maximum duty of each type of MOSFET according to the design procedure in Chapter 6. To conduct the comparison without any influence from ESR and ESL, the verification is conducted by simulation based on the schematic in Fig. 7. The gate driving voltages are set to proper voltages according to the datasheet [39-40], minimizing the influence of on-resistance of the power device.

Table 10. Simulation parameters for output power comparison

Parameter	Symbol	Si-MOSFET	SiC-MOSFET
Gate voltage	v_{dr}	16V	18V
Phase angle	φ	0°	0°
Duty	D	0.4555	0.4825
Input voltage	V_I	400V	400V
Load resistance	R	50Ω	50Ω
External capacitor	C_{ex}	0F	0F
Linearized Parasitic Capacitance	C_{dseq}	455pF	72pF
Total inductor	L	468.103uH	468.103uH
Resonant capacitor	C_r	7.782nF	7.704nF
Loaded quality factor	Q_L	5	5
ESR	r_{ESR}	0Ω	0Ω
ESL	L_1~L_8	0H	0H

The simulated waveform of Si-MOSFET and SiC-MOSFET are shown in Fig. 21 and Fig. 22. The ZVS operations are successfully conducted by each type of MOSFET with the minimum shunt capacitance and maximum duty. The simulated maximum output powers are listed in Table 11. The compared result indicates that the maximum output power obtained by SiC-MOSFET is higher than that by Si-MOSFET.

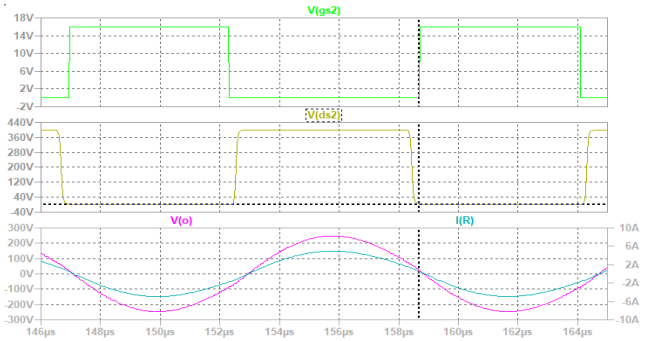


Fig. 21 Simulated waveform with maximum duty by Si-MOSFET

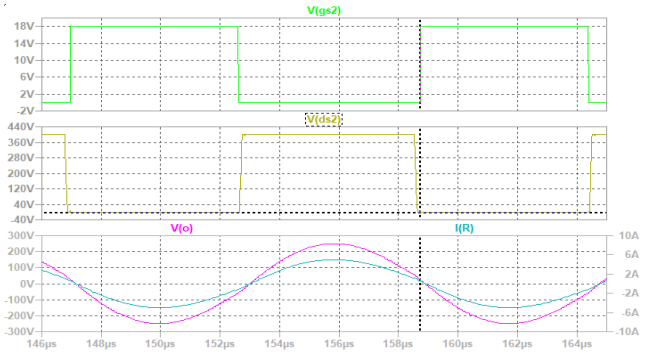


Fig. 22 Simulated waveform with maximum duty by SiC-MOSFET

Table 11. Simulated output power comparison

Power MOSFET (650V/30A)	Si-MOSFET R6530ENZ4	SiC-MOSFET SCT3080AL
Maximum Output Power	621.24W	632.38W

The reason for the result is that the parasitic capacitance of the SiC-MOSFET is much smaller than that of the Si-MOSFET. Thus, under the ZVS condition, the necessary time for the parasitic capacitance's charge or discharge is shorter, resulting in a larger maximum duty. Then, by designing with a larger maximum duty, a higher maximum output power can be obtained. From this result, it can be inferred that in the design of the class-D inverter, the power MOSFET with smaller nonlinear parasitic capacitance can obtain higher output power under the ZVS condition.

9. Conclusion

This paper verified the output power characteristics of the class-D inverter under the ZVS condition. The condition for obtaining high output power under the ZVS condition is analyzed as high input DC voltage, 0° output current phase angle (class-DE mode), and large duty cycle. The analysis is verified by both Si-MOSFETs and SiC-MOSFETs via simulation and experiment. The difference of maximum output power between the Si-MOSFETs and SiC-MOSFETs is also analyzed and verified. The simulated result indicates that the power MOSFET with smaller nonlinear parasitic capacitance can obtain higher output power under the ZVS condition.

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Yi Xiong received a B.S. degree in Electrical Engineering and the Automation in Wuhan, China in 2010, and an M.S. degree in Electronic Information Engineering at Gunma University, Kiryu, Japan in 2018, respectively. He is currently working toward a Ph.D. degree in Electrical Engineering at, the Department of Engineering of Nagoya University, Nagoya, Japan. His research interest mainly includes the analysis of high-frequency high-power inverters.

Thilak Senanayake received his B.S degree from the University of Colombo, Sri Lanka, in 1991., M.E., and Ph.D. degrees in Electronics Engineering from the Kyushu University, Japan, in 2001,2004, respectively. From 2004-2005 he was associated with the Graduate School of Information Science and Electrical Engineering as a Visiting Researcher. From 2005 to 2015, he was a Research Scientist at Toyota Central Research and Development Laboratory Inc., and DENSO Corporation, Japan. From 2015 to 2019, he was a Research Scientist at Power Electronics Laboratory, University of Tsukuba, Japan. Since 2019 he has been with Nagoya University, Japan, where he is currently a Research Scientist in the Power Electronics Laboratory involved in wireless power transfer and application of new wide-band-gap semiconductor devices (SiC/GaN).

Daisuke Arai received his M.S. and Ph.D degrees in Electronic Engineering from the University of Tokyo, Tokyo, Japan in 1996 and 2000 respectively. From 2000 to 2005, he worked on the development of IGBTs and super junction MOSFETs at Fujielectric Co., Ltd., Matsumoto, Japan. From 2005 to 2007, he worked on the development of high-voltage LDMOS at ON Semiconductor CO., LTD., Kitakata, Fukushima, Japan. From 2007 to 2012 he worked on the development of middle voltage power MOSFETs for automotive at Renesas Electronics CO., LTD., Gumma, Japan. From 2014 to 2019 he worked on the research on the switching mechanism of super junction MOSFETs at Shindengen CO., LTD., Saitama, Japan. Since 2020 he has been with Nagoya University, Japan, where he is currently investigating the switching mechanism of GaN power devices.

Jun Imaoka received his M.S. and Ph.D. degrees in Electronic Function and System Engineering from Shimane University, Matsue, Japan, in 2013 and 2015, respectively. From October 2015 to March 2018, he worked at Kyushu University, Fukuoka, Japan as an Assistant Professor. From April 2018 to March 2021, he was an Assistant Professor at Nagoya University, Nagoya, Japan. He is currently an Associate Professor at the Institute of Materials and Systems for Sustainability (IMaSS), Nagoya University His research interests include the design of integrated magnetic components, modeling for high-power-density power converters, thermal management for power converters, magnetic material application, and EMI of switching power supply. He is a member of the Institute of Electrical Engineers of Japan (IEEJ).

Masayoshi Yamamoto received his M.S. and Ph.D. degrees in science and engineering from Yamaguchi University, Yamaguchi, Japan in 2000 and 2004 respectively. From 2004 to 2005, he was with Sanken Electric Co., Ltd., Saitama, Japan. From 2006 to 2017, he was with the Interdisciplinary Faculty of Science and Engineering at Shimane University, Japan, as an Associate Professor. He is currently a Professor at the Institute of Materials and Systems for Sustainability (IMaSS), Nagoya University, Japan. His research interests include power supply for HEV (boost converter, buck converter, 3-phase inverter, digital control), charging system for EV, LED illumination system for a tunnel, EMI of switching power supply, and wireless power transfer. He is a member of the Institute of Electrical Engineers of Japan (IEEJ).