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PAPER

Systematic Offset Voltage Reduction Methods Using Half-Circuit of Input Stage in the Two-Stage CMOS Operational Amplifiers and Comparators

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SUMMARY In this study, we propose the systematic offset voltage reduction method considering the channel length modulation effect for the two-stage CMOS operational amplifiers (Op-Amps) and comparators. The proposed method employs the half-circuit of the input stage in two-stage Op-Amps as the output stage. Using the proposed method, each terminal voltage of the MOS transistors in the input and output stages is aligned, and the channel length modulation effect can be ignored. To generalize the proposed method, we applied the proposed method to Op-Amps with the cascode active load and differential difference amplifier. The systematic offset voltage was evaluated and compared by simulation using HSPICE with TSMC 0.18 μm model parameters. Consequently, we confirmed that the proposed method can reduce the systematic offset voltage by 95% or more.

key words: *CMOS analog circuit, low offset voltage*

1. Introduction

Recently, the number of sensors mounted in electric vehicles as well as mobile and wearable devices has been increasing. These sensors have become more sophisticated, and the safety of their systems has improved. Therefore, various analog circuits for processing signals obtained from sensors are becoming increasingly important[1]. Operational amplifiers (Op-Amps) are indispensable in fabricating these analog circuits, and various types have been proposed. In these Op-Amps, the two-stage Op-Amp, which comprises a differential pair and common source amplifier circuit, is often used in various circuits because of its simple architecture and relatively easy design[2]–[4]. For example, in [2], this Op-Amp is used as an auxiliary amplifier for the regulator in the BGR circuit.

Furthermore, one of the performance indicators of Op-Amp is the offset voltage. Naturally, a large offset voltage significantly degrades the performance of the entire circuit and is therefore often noted as an essential performance indicator[5].

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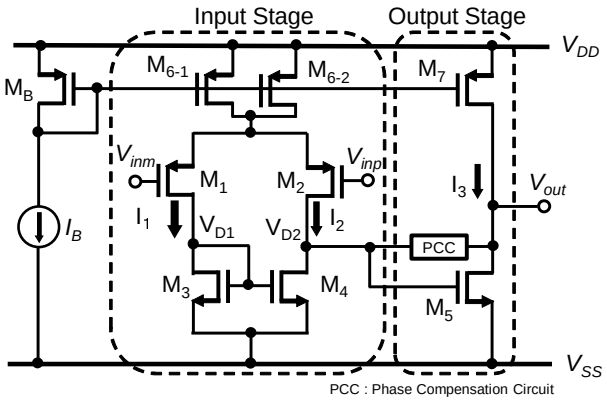


Fig. 1: Two-stage CMOS Op-Amp

The offset voltage can be divided into two types: random and systematic offset voltages[6]. The random offset voltage is typically caused by device mismatch in the fabrication process. In many cases, the mismatch is reduced by using various techniques in mask layout design, such as common-centroid and device placement, based on the characteristics of the fabrication process to reduce the mismatch[7], [8]. However, the systematic offset voltage is caused by the mismatch that occurs in the design of the differential pair[9]. In CMOS Op-Amps, a major source of systematic offset voltage is the channel length modulation effect[6].

For random and systematic offset voltages, several methods have been proposed to reduce the offset voltage using circuit techniques[10]–[15]. The first method is to reduce the offset voltage using a CMFB circuit[10], [11]; the second method is to reduce the offset voltage using a chopper technique[12], [13]. Another method is to add a switch use a clock signal, and store the offset voltage in a capacitor. The capacitor is then used to cancel the offset voltage[14]. Although the above methods are effective, problems such as the need for a clock and the use of many transistors and capacitors must be overcome. Therefore, the chip area and design complexity may be increased. Another design method that has been proposed is to adjust parameters related to the offset voltage; however, the reduction is limited[15].

The required offset voltage depends on the application. Recently, the offset voltage of Op-Amp is several tens mi-

crovolt (μV) level. The Ref. [4], published in 2019, reported a systematic offset voltage of 50.8 μV for the two-stage Op-Amp used in medical applications. Especially, a typical biomedical application requires the offset voltage to sub-nano volt (nV) level for ECG signal sensing[16]. To achieve the sub-nano volt level offset voltage, it is necessary to improve not only the external circuit but also the design method. Therefore, it is important to design a low-offset Op-Amp with a simple and low chip area.

In this study, we propose a new method to reduce the systematic offset voltage in two-stage Op-Amps, as shown in Fig. 1. The Op-Amp shown in Fig. 1 can be used as a comparator by removing the phase compensation circuit[17]. In addition, a design method to reduce the systematic offset voltage has already been established for this Op-Amp[18]. However, the channel length modulation effect is not considered in this design method; a relatively large offset voltage can be observed. Conversely, because the method proposed in this study considers the influence of the channel length modulation effect, it can be expected to have an improvement effect compared to the conventional design method.

This paper is organized as follows. In Section 2, using the circuit in Fig. 1 as an example, the problems with the conventional design method to reduce the systematic offset voltage are explained. Section 3 describes the proposed method of reducing the systematic offset voltage using the circuit in Fig. 1 as an example. Thereafter, the proposed method is extended to a general two-stage Op-Amps. We apply the proposed method to other circuit. In Section 4, we compare the performance of both the conventional and proposed design methods by SPICE simulation. Finally, Section 5 presents a summary of this paper.

2. Conventional Method for Reducing Systematic Offset Voltage and Its Problem

This section first describes the conventional method for reducing the systematic offset voltage, using the Op-Amp shown in Fig. 1 as an example and then refers to the problems of the method.

2.1 Ploblem of Conventional Method

The drain-to-source current I_{DS} of a MOS transistor operating in the saturation region is expressed as follows[19]

$$I_{DS} = \frac{K}{2}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \tag{1}$$

where K is the transconductance parameter, and this value is proportional to the channel width W and inversely proportional to the channel length L. V_{TH} is the threshold voltage and λ is the channel length modulation coefficient. For small value λ, Eq. (1) can be approximated as follows

$$I_{DS} \approx \frac{K}{2}(V_{GS} - V_{TH})^2. \tag{2}$$

In Fig. 1, we assume that the λ is considerably small and Eq. (2) is satisfied, L and W of M_1 and M_2 are equal, L and W of M_3, M_4, and M_5 are equal, and L and W of M_B, M_{6-1}, M_{6-2}, and M_7 are also equal. Furthermore, we assume that the input voltages, V_{inm} and V_{inp}, are on the bias and have equal voltage. In this case, M_B, M_{6-1}, M_{6-2}, and M_7 constitute a current mirror; their I_{DS} are all equal, and their value is I_B. Furthermore, because the V_{GS} of M_1 and M_2 are equal, $I_1 = I_2 = I_3 = I_B$. Therefore, $V_{GS3} = V_{GS4} = V_{GS5} = V_{DS3}$ $(= V_{D1})$ in M_3, M_4, and M_5. Because $V_{GS5} = V_{D2}$ from Fig. 1, V_{GS} and V_{DS} of the relative left and right MOS transistors in the input stage are equal. Therefore, the systematic offset voltage is reduced when the current density of the transistors in the input and output stages are the same.

However, in general, the channel length modulation effect is marked in fine manufacturing processes, and the λ of Eq. (1) cannot be ignored. We simulated and confirmed λ of the minimum channel length devices in the 0.18 μm and 0.6 μm CMOS process, and the value of λ in the 0.18 μm CMOS process was observed approximately 2.3 times higher than that of the 0.6 μm CMOS process. To overcome this, we should use long-channel devices for the reduction of the systematic offset voltage. However, it has a problem with increasing the chip area. The method proposed in Section 3 can reduce the systematic offset voltage even when designed with short-channel devices. Therefore, the reduction of the systematic offset voltage versus the chip area is highly effective, and area efficiency is improved compared to the conventional method.

2.2 Cause of Systematic Offset Voltage

The offset voltage is evaluated at the value that appears on the output point when in the bias condition. In this bias condition, the input voltages of Op-Amps biased $(V_{DD} + V_{SS})/2$. In this section, we will focus on the MOSFETs voltage and current from the circuit shown in Fig. 1. The principle of the offset voltage generated on the output point of a differential pair when V_{D1} and V_{D2} are not in equilibrium is explained.

First, we consider the bias condition, i.e., when V_{GS} of M_1 and M_2 shown in Fig. 1 are equal. In this case, all MOSFETs are operating in the saturation region, and V_{GS} of M_3 and M_4 and V_{DS} of M_3 are equal ($V_{GS3} = V_{GS4} = V_{DS3}$). If $V_{D1} = V_{D2}$ is satisfied, the V_{GS} and V_{DS} of each MOSFET pair in the input stage are equal. In particular, the differential pair is in equilibrium and is not affected by the channel length modulation. Next, we aligned the W/L of M_{6-1}, M_{6-2} and M_7 to satisfy $V_{D1} = V_{D2}$ assumed in this explanation. This is the conventional design method, which allows $V_{D1} = V_{D2}(V_{GS5})$.

However, using Eq. (1), we can find a problem with the above design method. When the input stage is in equilibrium, because $V_{D1} = V_{D2}$, we obtain $V_{GS3} = V_{GS5}$. Using Eq. (1), we have the following equation.

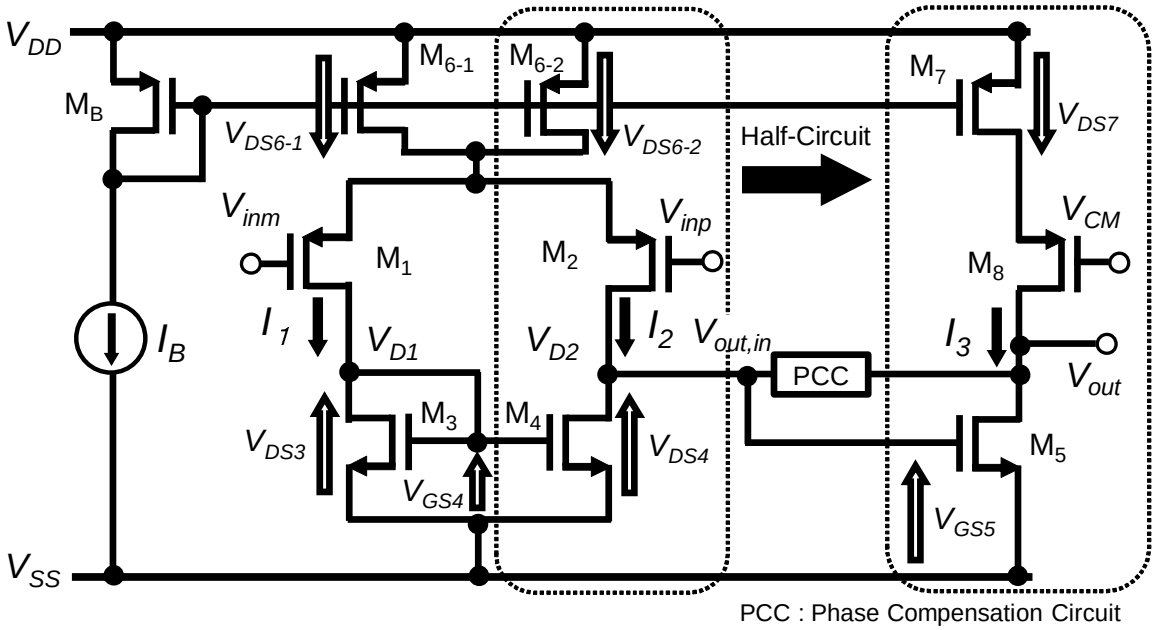


Fig. 2: Proposed two-stage CMOS Op-Amp

$$\sqrt{\frac{2I_1}{K(1+\lambda_n V_{DS3})}}+V_{TH}=\sqrt{\frac{2I_3}{K(1+\lambda_n V_{DS5})}}+V_{TH}. \quad (3)$$

Here, considering that random variation is negligible, the K and V_{TH} on both sides are equal. Therefore, the equation can be transformed as follows.

$$\frac{I_1}{1+\lambda_n V_{DS3}}=\frac{I_3}{1+\lambda_n V_{DS5}}. \quad (4)$$

Furthermore, we can assume that $I_1 = I_{DS6-1}$ and $I_3 = I_{DS7}$ in equilibrium. Thus, we can obtain the following equation.

$$\frac{1+\lambda_p V_{DS6-1}}{1+\lambda_n V_{DS3}}=\frac{1+\lambda_p V_{DS7}}{1+\lambda_n V_{DS5}}. \quad (5)$$

From the previous explanation, the differential pair is observed to be in equilibrium when the above equation is satisfied. However, the number of vertical stacking of the input and output stages is different. To satisfy the above equation, the V_{DS} of M_1 and M_2 of the differential pair constituting the input stages must be 0 V. Therefore, all MOSFETs is not operating in the saturation region, which contradicts the previous explanation. In particular, the above equation shows that the differential pairs are not at equilibrium in the Conventional Op-Amp, resulting in a systematic offset voltage generated.

In addition, Eq. (5) shows that equality cannot be satisfied even when the channel length modulation effect is reduced by using a long-channel device. This is because the value of λ does not become completely 0, even with the use of long-channel devices, indicating that the channel length modulation effect remains.

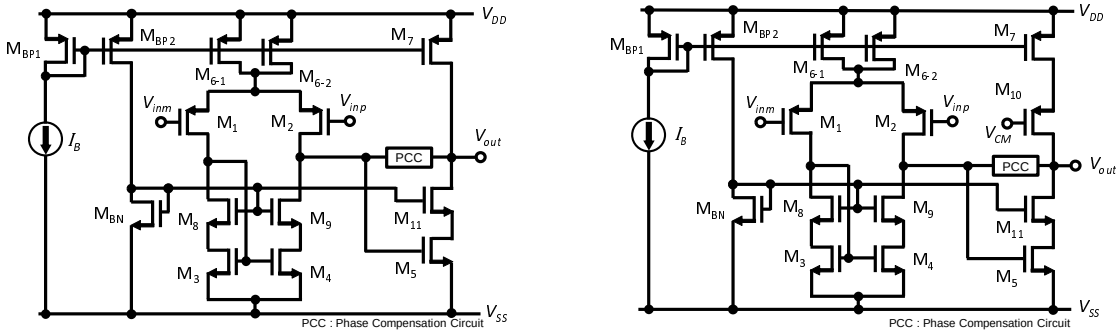
3. Systematic Offset Voltage Reduction Method Considering Channel Length Modulation

3.1 Proposed Circuit

Figure 2 shows the proposed circuit. Comparing the input and output stages in the circuit shown in Fig. 2, it can be observed that the output stage is a half-circuit of the input stage. In the case of Fig. 2, the proposed method is only the addition of M_8 in the output stage. The L and W of M_8 are set equal to those of M_1 and M_2, and we can apply the common-mode voltage (V_{CM}) of M_1 and M_2 to the gate terminal of M_8. The addition of M_8 ensures the number of vertically stacked MOS transistors equal and the circuit configuration of the input and output stage in bias condition equal. Therefore, it satisfies $V_{DS6-1} = V_{DS6-2} = V_{DS7}$ and $I_{DS6-1} = I_{DS6-2} = I_{DS7}$. Hence, we can obtain $I_1 = I_2 = I_3$, $V_{GS3} = V_{GS4} = V_{GS5} = V_{DS3}$ $(= V_{D1})$, and $V_{D1} = V_{D2}$. Consequently, the systematic offset voltage can be reduced even when the channel length modulation effect is not ignored.

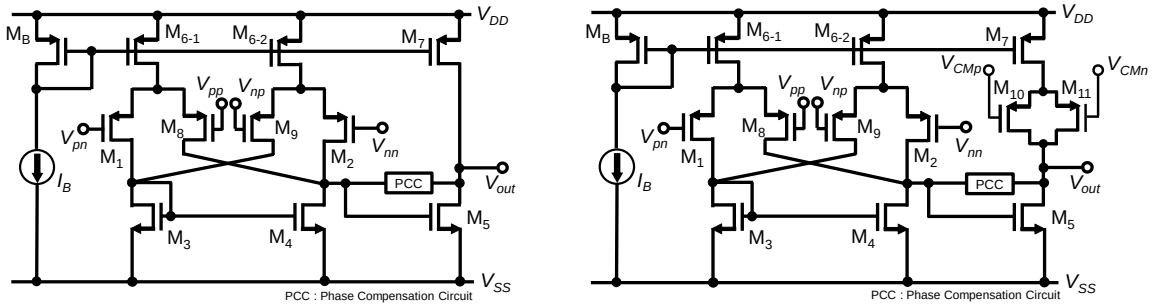
3.2 Generalization of the Proposed Method

In the previous section, we discussed the two-stage Op-Amp shown in Fig. 1 and described a method for reducing the systematic offset voltage considering the channel length modulation. The proposed method, which uses the half-circuit of the input stage as the output stage in the Op-Amp, can be generalized. Using this method, each terminal voltage in the equilibrium state of the input stage can be generated and used to maintain the equilibrium state of the input stage,



(a) Conventional **(b)** Proposed

Fig. 3: Two-stage CMOS Op-Amp with cascode active load



(a) Conventional[21] **(b)** Proposed

Fig. 4: Two-stage CMOS differential difference amplifier (DDA)

thereby reducing the systematic offset voltage.

Examples of circuits using the proposed method are shown in Figs. 3(b) and 4(b). Figure 3(b) shows a circuit example using a cascode active load, and Fig. 4(b) shows a differential difference amplifier (DDA) [20], [21]. In both cases, the half-circuit of the input stage is used for the output stage, and the proposed method is expected to reduce the systematic offset voltage.

4. Evaluation by Simulation

In this section, to confirm the effectiveness of the proposed method, the Op-Amps using the conventional and proposed methods are evaluated and compared through the SPICE simulation. All Op-Amps were designed with the TSMC 0.18 μm CMOS model parameters and simulated using the HSPICE.

4.1 Simulation Condition

Table 1 shows the design values of the circuits shown in Figs. 1, 2, 3, and 4. The back-gate terminal of the PMOS and NMOS transistors are connected to V_{DD} and V_{SS}, respectively. In the case of DDA shown in Fig. 4(b), V_{CMp} and V_{CMn} are the same voltage. In addition, $V_{imp} = V_{pp} = V_{nn}$ and $V_{inm} = V_{np} = V_{pn}$. In particular, the output of DDA is $V_{out} \approx A(V_{inp} - V_{inm})$, as in two-stage CMOS Op-Amp shown Fig. 1. we use 25 °C as the typical temperature.

About the design parameters of the proposed circuit shown in Fig. 2, V_{out} may be close to $V_{out,in}$ owing to the relation that the output stage constitutes a half-circuit of the input stage. Because both power supplies (±0.9 V) are used in this design, we attempted here to design $V_{out,in}$ to be almost 0 V. Specifically, we used the following equation

$$V_{GS3} = \sqrt{\frac{2I_1}{K(1+\lambda V_{DS3})}} + V_{TH3}. \tag{6}$$

We obtained $W = 0.394$ μm, and consequently, adopted $W = 0.4$ μm. In this case, L of the NMOS transistor is set to 1.8 μm. Similarly, for the PMOS transistor, $L = 0.6$ μm was used in the design. Consequently, we derived $W = 4.0$ μm.

Next, we will discuss evaluation circuits and methods related to the offset voltage. The offset voltage is evaluated as the input-referred offset voltage, which is defined as the input level that results in $V_{out} = 0$. The input-referred voltage $V_{OS,in}$ is defined [19]

$$V_{OS,in} = \frac{|V_{OS,out}|}{A_V} \tag{7}$$

where A_V is the voltage gain of Op-Amps, and $V_{OS,out}$ is the output voltage when V_{inp} and V_{inm} set to bias condition.

In this study, we employed two types of evaluation circuits: one in which the output terminal V_{out} was open (Evaluation 1), and another in which V_{out} was connected to V_{inm}

(Evaluation 2). In both evaluation circuits, a DC voltage source V_{in} is connected to the V_{inp}. In Evaluation 1, the V_{out} is open and set to $V_{inm} = 0$, and we can observe the variation in output voltage V_{out} as V_{in} is swept from −10 mV to +10 mV. In this case, to evaluate the input-referred offset voltage, the input voltage when $V_{out} = 0$ was observed. In Evaluate 2, we employed the consist of the Op-Amp voltage follower. In this case, we observed the V_{out} when $V_{in} = 0$ as the input-referred offset voltage.

4.2 Simulation Result

Table 2 shows V_{DS} of each MOSFET when $V_{inp} = V_{inm} =$ 0 V. In the conventional Op-Amp (Fig. 1), V_{DS6-1} and V_{DS7} are different because the number of vertically stacked MOS transistors is different between the input and output stages. Furthermore, V_{DS3} and V_{DS5} are not equal; thus, the differential pair is not in equilibrium, and a systematic offset voltage is generated. However, in the circuit using the proposed method (Fig. 2), V_{DS6-1} and V_{DS7} are the same voltages owing to the addition of PMOS transistor M8. In addition, V_{DS5} and V_{DS3} are equal; therefore, the current density in the input and output stages is the same. Thus, we can confirm that the differential pairs are at equilibrium in the proposed circuit.

Figure 5 show the simulation results of the DC analysis. In all MOSFETs operate in the saturation region, we can express the output range of the proposed circuit shown in Fig. 2 as follows:

$$V_{SS} + V_{ONn} < V_{out} < V_{CM} + V_{THp} \tag{8}$$

where V_{ONn} is the overdrive voltage ($V_{ONn} = V_{GSn} - V_{THn}$) of NMOS transistors. In this range, the proposed circuit can reduce the systematic offset voltage effectively. On the other hand, when $V_{out} > V_{CM} + V_{THp}$, the PMOS transistor M_7 operates in saturation region but M_8 operates in the linear region. When operating in this range, the proposed circuit has the same systematic offset voltage and output range as the conventional circuit.

In Fig. 5, when $V_{out} = 0$, the input voltage V_{in} is close to 0V, which confirms that the proposed method reduces the input-referred offset voltage. These results of the input-referred offset voltage are summarized in Table 3. While the offset voltage was 124 μV for the Op-Amp shown in Fig. 1, it was 4.54 μV for the Op-Amp shown in Fig. 2, confirming the reduction rate of 96.3%. Similarly, the reduction rate of 95% or more was confirmed in the case of Figs. 3 and 4.

In Table 3, we can see that little difference between Evaluation 1 and Evaluation 2. The reason for this is the step size of DC analysis was set to 100 nV. Consequently, the error between evaluation circuits is minimal.

4.3 Influence of PVT Variation

We evaluated corner conditions of FF (fast NMOS and fast PMOS), FS (fast NMOS and slow PMOS), SS (slow NMOS and slow PMOS), SF (slow NMOS and fast PMOS), and TT (typical) for this analysis. We used temperatures of −50°C, −25°C, 0°C, 25°C, 50°C, 75°C, and 100°C. In addition, the power-supply voltages of ±0.8 V, ±0.9 V, and ±1.0 V were used in this simulation.

Table 4 shows the maximum and minimum values of the input-referred offset voltage of the conventional and proposed circuit (Figs. 1 and 2) with PVT variations. We observed values in Table 4 from the results of DC analysis with Evaluation 1 and Evaluation 2.

On the other hand, we can consider the influence of PVT variation from Eq. (7). Figures 6 and 7 show the temperature dependence of the output offset voltage and voltage gain each PVT condition. Figure 8 shows the input-referred offset voltage calculated from Eq. (7) using the values obtained from Figs. 6 and 7. We will discuss the PVT conditions showing the maximum and minimum values referring to Table 4 and Figs. 6, 7, and 8.

4.3.1 Coner Condition Showing Maximum Values

We will discuss the corner conditions which we observed the maximum value of the input-referred offset voltage. At the SS corner, the absolute value of the threshold voltage of the MOSFET increases, and the transconductance parameter K decreases compared with the TT corner. This variation causes an increase in the V_{DS5} (output offset voltage $V_{OS,out}$) in both circuits. According to Fig. 6, in the conventional circuit, the $V_{OS,out}$ at the TT corner is a positive value, which means that the absolute value of the $V_{OS,out}$ increases at the SS corner. On the other hand, in the proposed circuit, the $V_{OS,out}$ at the TT corner is a negative value, which means that the absolute value of the $V_{OS,out}$ decreases at the SS corner. In contrast to the SS corner, the absolute value of the $V_{OS,out}$ in Fig. 2 increases at the FF corner. Consequently, the input-referred offset voltage shows its maximum value at the SS corner in the conventional circuit and the FF corner in the proposed circuit.

4.3.2 Corner Condition Showing Minimum Values

We will discuss the corner conditions which observed the minimum value. We observed the voltage gain is highest at the TT corner shown in Fig. 7. This reason is as follows; at the FF corner, the voltage gain significantly decreases because the λ of the MOSFET increases, and at the SS corner, the voltage gain decreases because the transconductance parameter K of the MOSFET in the output stage decreases. Consequently, for both circuits, the minimum values of the input-referred offset voltage were observed at the TT corner.

4.3.3 Output Offset Voltage with Variation of Power-Supply Voltages

We will discuss the output offset voltage with respect to V_{DD} and V_{SS} (the power-supply voltages) variation. When the power-supply voltages increase, the $V_{OS,out}$ of both conventional and proposed circuits decreases because the V_{DS7}

Table 1: Design parameter of the conventional and the proposed circuits

	NMOS W/L	PMOS W/L	I_B	V_{DD}	V_{SS}
Fig. 1 and Fig. 2 Figs. 3(b) and 3(a) Figs. 4(a) and 4(b)	0.4/1.8 μm/μm	4.0/0.6 μm/μm	5 μA	0.9 V	−0.9 V

Note: In Figs. 3(a) and 3(b), the channel length of M_{BN} is 3.5 times, and the channel width of M_8, M_9 and M_{11} is 2 times.

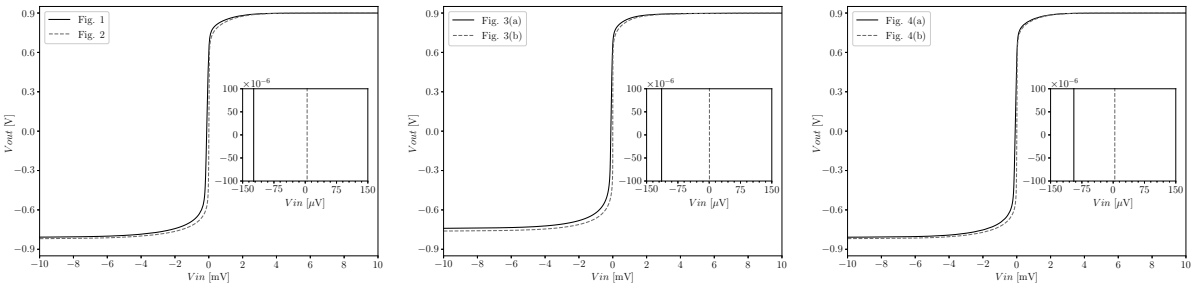


Fig. 5: Simulation results of DC analysis

Table 2: Each V_{DS} of MOS transistors at the bias condition

	Fig. 1	Fig. 2
V_{DS6-1}	236 mV	236 mV
V_{DS7}	291 mV	236 mV
V_{DS3}	0.791 V	0.791 V
V_{DS5}	1.51 V	0.791 V

Table 3: Input-referred offset voltages

	Figs. 1 and 2	Fig. 3	Fig. 4
Conventional			
Evaluation 1	124 μV	114 μV	94.2 μV
Evaluation 2	124 μV	114 μV	94.2 μV
Proposed			
Evaluation 1	4.54 μV	0.584 μV	3.86 μV
Evaluation 2	4.55 μV	0.580 μV	3.86 μV
Reduction Rate			
Evaluation 1	96.3%	99.5%	95.9%
Evaluation 2	96.3%	99.5%	95.9%

absorbs the increase in the power-supply voltages. This means that V_{DS7} increases. Therefore, the $V_{OS,out}$ of both circuits becomes low with increasing the power-supply voltages. As mentioned earlier, the $V_{OS,out}$ of the conventional and proposed circuit shows positive and negative values, respectively. As the results, we observed the maximum value at ±0.8 V in the conventional circuit and ±1.0 V in the proposed circuit. Similarly, the minimum value was observed at ±1.0 V in the conventional circuit and ±0.8 V in the proposed circuit.

4.3.4 Temperature Dependence of Voltage Gain and Output Offset Voltage

We will discuss the temperature dependence. The change in the voltage gain (the denominator of Eq. (7)) with a change of temperature is more significant because it is larger than the change in the $V_{OS,out}$ (the numerator of Eq. (7)) with a change of temperature.

In addition, the voltage gain of both circuits shows a monotonic decrease with rising temperature shown in Fig. 7. Therefore, the input-referred offset voltage of the conventional and proposed circuits shows a maximum value at 100°C. Similarly, the minimum value of the conventional circuit was observed at −50°C.

On the other hand, the minimum value of the proposed circuit was observed at 75°C. This is because the $V_{OS,out}$ of the proposed circuit increases with rising temperature, transitions from negative to positive values around 75°C, and approaches 0 V shown Figs. 6 and 8.

4.3.5 Summary of PVT Variation

In our analysis of the PVT conditions, we used the output offset voltage and voltage gain as evaluation metrics. Comparing Table 4 with Fig. 8, we see that the same PVT conditions correspond to the minimum value in Fig. 1 and the maximum and minimum values in Fig. 2. However, the PVT condition corresponding to the maximum value in Fig. 1 is different. This is because that the $V_{OS,out}$ saturates in the conventional circuit at the SS, ±0.8 V.

In addition, Fig. 9 shows the values from Evaluation 2, which shows the same PVT conditions as in Table 4. Evaluation 2 also confirms that all PVT conditions with maximum and minimum values were derived for the same reasons as mentioned above. Here, the use of feedback allows for easy observation of the offset voltage, making it useful for chip measurement.

From Table 4, we can conclude that the input-referred offset voltages of the proposed circuit remain significantly lower than those of the conventional circuit, even when PVT variation is applied.

Table 4: Results of PVT variation

	Fig. 1		Fig. 2	
Evaluation circuit	Eval. 1	Eval. 2	Eval. 1	Eval. 2
Typical	124 μV @ TT, ±0.9 V, 25°C	124 μV	4.54 μV @ TT, ±0.9 V, 25°C	4.55 μV
Maximum	310 μV @ SS, ±0.8 V, 100°C	311 μV	21.7 μV @ FF, ±1.0 V, 100°C	21.7 μV
Minimum	88.4 μV @ TT, ±1.0 V, −50°C	88.4 μV	23.6 nV @ TT, ±0.8 V, 75°C	13.8 nV

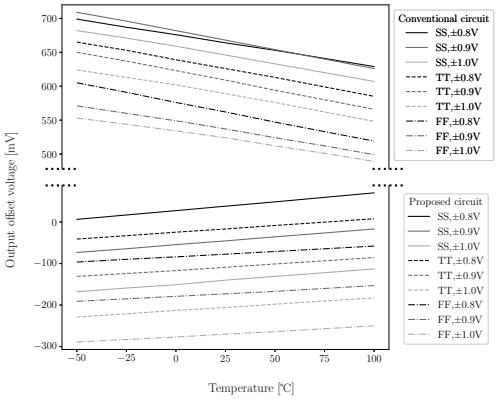


Fig. 6: Temperature dependence of the voltage gain

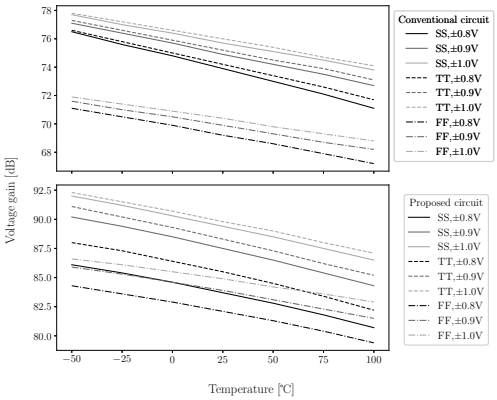


Fig. 7: Temperature dependence of the voltage gain

Table 5: Offset voltage when changing element values of MOSFETs with Evaluation 1

	Fig. 1	Fig. 2	FoM of Fig. 1	FoM of Fig. 2
Case 1	124 μV	4.54 μV	2.05×10^{-3}	8.61×10^{-5}
Case 2	3.58 μV	0.222 μV	1.45×10^{-2}	1.05×10^{-3}
Case 3	4.75 μV	0.205 μV	7.39×10^{-3}	4.46×10^{-4}

Note: Case 1 is the result when we use the element value of MOSFETs in Table 1. Case 2 is when we used $L = 10\ \mu m$, and Case 3 is when we used 10 times the element value of MOSFETs in Table 1.

4.4 Comparison with long-channel devices

Table 5 shows the simulation results of the input-referred offset voltages when the channel length (MOSFET element value) is changed. Using $L = 0.6\ \mu$m for PMOS and $L = 1.8\ \mu$m for NMOS as reference values (Case 1), table 5 shows the case where $L = 10\ \mu$m for MOSFETs (Case 2) and the case where L and W are 10 times the reference values (Case 3). The input-referred offset voltage of the conventional circuit in the case 2 is significantly reduced to 3.58 μV compared to that in case 1. This confirms that the channel length modulation effect has been reduced. The proposed circuit also shows a similar significant reduction.

In addition, the input-referred offset voltage of the conventional circuit in Case 3 is almost equal to that of the proposed circuit in Case 1. Therefore, the proposed method has an equivalent effect on the input-referred offset voltage when the channel length is set to 10 times in the manufacturing process used in this study.

Furthermore, we calculated scores of the relationship between the element values of MOSFETs and the input-referred offset voltage as the Figure of Merit(FoM). We determined the FoM given by

$$FoM := V_{OS,in} \times (W_p L_p n_p + W_n L_n n_n) \tag{9}$$

where W_p and W_n are the channel width of PMOS and NMOS transistors respectively. Similarly, L_p and L_n are the channel length of PMOS and NMOS transistors, and n_n and n_p are the number of PMOS and NMOS transistors used

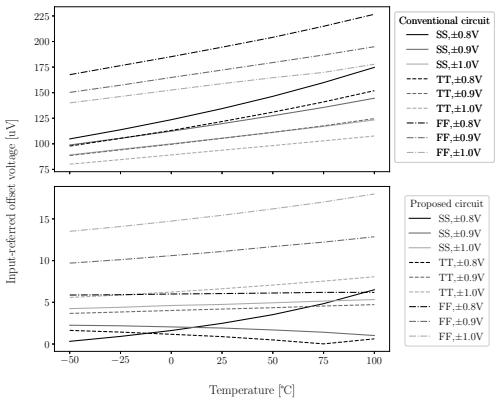


Fig. 8: Results of calculations for input-referred offset voltage

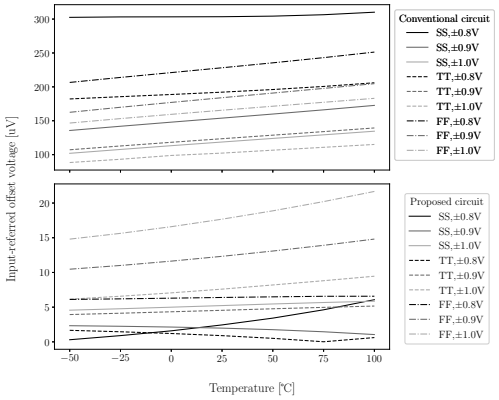


Fig. 9: Results of input-referred offset voltage with Evaluation 2

in the Op-Amp. In the case of this FoM, we can evaluate that the smaller value has a low chip area and low-offset voltage. In all cases, we confirm that the FoM with the proposed method was smaller than those obtained with the conventional method. In addition, we compare the FoM of Fig. 1 in the case 3 and the FoM of Fig. 2 in the case 1. As a result, despite both of the circuits having almost the same input-referred offset voltages, we confirmed that the FoM is drastically improved by using the proposed method.

5. Conclusion

In this study, we proposed a method to reduce the systematic offset voltage considering the channel length modulation effect for the two-stage CMOS Op-Amps and Comparators. In the proposed method, a half-circuit of the input stage in the Op-Amp was used as the output stage. By employing the proposed method, the differential pair can be equilibrated considering the channel length modulation effect, and the systematic offset voltage can be reduced.

The systematic offset voltage was evaluated and compared by simulation using the HSPICE with the TSMC 0.18 μm model parameters. The offset voltage of the Op-Amps using the proposed method was considerably small compared with that using the conventional method. As a result, we confirmed the reduction of the systematic offset voltage versus the chip area is highly effective.

Only the systematic offset voltage is considered in the proposed method; however, in future studies, the offset voltage owing to random variation should be considered in the actual mass production.

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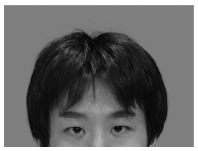

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