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LETTER

GNN-Opt: Enhancing Automated Circuit Design Optimization with Graph Neural Networks

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SUMMARY We introduce ”GNN-Opt,” a method that adapts ”DNN-Opt’s ” machine learning approach for analog circuit design, particularly op-amp sizing. By utilizing Graph Neural Networks, GNN-Opt demonstrates superior efficiency in transferring design knowledge across similar topologies, accelerating to achieve higher FoM with same simulation times.
key words: *Analog Integrated Circuits Design, Design Automation, Machine Learning, Deep Reinforcement Learning*

1. Introduction

Machine learning, particularly Deep Neural Network (DNN) technologies, are revolutionizing analog circuit design by automating complex tasks like operational amplifier (opamp) sizing, a process traditionally seen as time-consuming due to the intricate nature of circuit schematics. The development of DNN-Opt[1], a method that combines particle swarm optimization (PSO) and Deep Deterministic Policy Gradient (DDPG), marks a significant advancement by dramatically increasing efficiency and speed in circuit design. This method can finalize opamp designs that meet specific gain requirements in just a few hundred steps, roughly under an hour, showcasing a remarkable improvement in convergence speed over previous methods. This efficiency is attributed to the effective training of the critic network and minimizing of the loss function, allowing for accurate design predictions in large search spaces in a short time. The criticsuccess of the system raises the possibility of extending this model to different circuit topologies, potentially reducing or even eliminating the need for time-consuming circuit simulations, which currently take over three seconds per run. This could lead to faster sizing processes and enable more complex topology synthesis requiring numerous iterations. Building on criticthe success of DNN-Opt, we introduce a variation named GNN-Opt, employing Graph Neural Networks (GNNs) for the critic network architecture. This adaptation enabled the application of models trained on NMOS differential amplifier circuit sizing to PMOS one with similar structures for example. The innovation demonstrated that critictraining transferred via the actor network alone could enhance the Figure of Merit (FoM) in PMOS differential to a significant degree. Remarkably, the GNN-Opt model, initially trained on NMOS differential pairs, achieved high FoM in sizing PMOS one from the early stages of actor network training, without the need to train its critic network. This efficiency was comparable to, if not better than, models trained from scratch on PMOS sizing, underscoring the potential of machine learning in broadening the scope and efficiency of analog circuit design.

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2. Methodology

2.1 DNN-Opt

DNN-Opt is a reinforcement learning based approach for sizing to meet given performance targets using HSPICE and other simulation tools. It criticincludes actor and critic networks, as well as a method for criticincreasing the number of training data the power of two using PSO. The training process is based on the following design flow and the calculation of the loss function using the mean squared error (MSE).

2.2 Graph Neural Networks

DNN-Opt does not offer a comprehensive description of its neural network architecture. However, it is presumed to employ a general Fully-Connected Neural Network (FCNN). criticFCNN cannot recognize the connection of components, such as MOS, capacitors, and resistors, moreover, FCNN, where the number of components is the number of inputs, outputs an error if the number of inputs also changes due to a change in the number of components, etc, so FCNN models become non-functional when there is a change in topology. Consequently, once trained FCNN models are typically discarded. criticTo utilize the trained models to other circuit topologies, it has recently become known that it is effective to treat circuit topology as a graph structure. Hanrui et al [2]. investigated the possibility of transferring from one topology to another by reusing trained models, and this was achieved with Graph Neural Networks (GNNs), where the transfered model was found to outperform FCNNs and untrained models in the FoM of two topologies.

3. Experiments

In this section, we perform sizing on the GNN-Opt critic network under the following four conditions to see if the knowledge transfer between different topologies works correctly. (1) criticTraining sizing using an initialized model with NMOS basic differential pair and common source shown

in Fig.1. (2) Sizing by critictrainsmitting the model critictrained in (1) to NMOS basic differential pair and common source again. (3) Sizing by critictrainsmitting the model critictrained in (1) to a PMOS basic differential pair and common source shown in Fig.2. (4) criticTraining sizing using the model initialized to PMOS basic differential pair and common source for comparison in (3). (1) and (4) are trained using the same method as DNN-Opt for both critic and actor, and (2) and (3) are trained only for actor, criticand training transfered critic model is frozen.

criticIn order to eliminate subjectivity, the FoM calculation method, criticparametrics measurement methods and minimum criticrequirements for the characteristics follow the method used in division 1 of the 2022 Operational Amplifier Design Contest in Tokyo Institute of Technology[3], and FoM is set to 0 if even one of the minimum requirements shown in Table 1, is not met. Although previous studies have verified the use of comparators and so on in addition to opamps, we focus here only on opamps. critic-This is because there is no published method of measureing parametrics for analog circuits other than opamps such as comparators, etc., and therefore, the results cannot be fully guaranteed. criticIn this experiment we used HSPICE for simulation for training critic networks and took 3 seconds per step, which occupied more than 90% of the total time. 10 random samplings and 150 searches were performed for each sizing topologies. These times were defined from the training time and memory throughput, because the DNN-Opt architecture does not allow for so many simulations because the number of data for training grows at the rate of squares.

Table 1 FoM and specifications that circuit must satisfy

evaluation item	terms
FoM	$\frac{\text{SR}\times\text{DCgain}\times\text{CMIR}}{\text{CC}}$
Current Consumption (CC)	50% or less
Power Consumption (= VDD×CC)	100mW or less
DC Gain	40dB or more
Phase Margin (PM)	45° or more
Gain Bandwidth Product (GB Product)	more than 1MHz
Input Referred Noise (IRN)	none
Slew Rate (SR)	0.1V/μs or more
Total Harmonic Distortion (THD)	1% or less
Common Mode Rejection Ratio (CMRR)	40dB or more
Power Supply Rejection Ratio (PSRR)	40dB or more at 0.1Hz
Output Voltage Range	5% or more
Common Mode Input Range (CMIR)	5% or more
Occupied Area	1mm^2 or less

3.1 Discussion

The results are as follows. First, we checked the critic and actor loss functions for (1) and (4) shown in Fig.3. The critic's loss function decreases with the number of simulations, indicating that critictraining is progressing, i.e., the design space is being correctly recognized. Most of the actor's loss functions are also stable at around 0.05 0.25, which confirms that the prediction is not far off from the critic's prediction. We can also confirm that criticthe FoM is increases as critic's

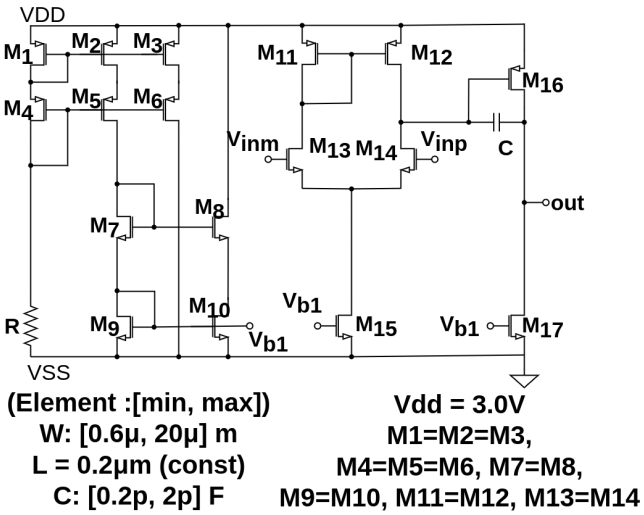

Fig. 1 criticNMOS differential pair and common source topology

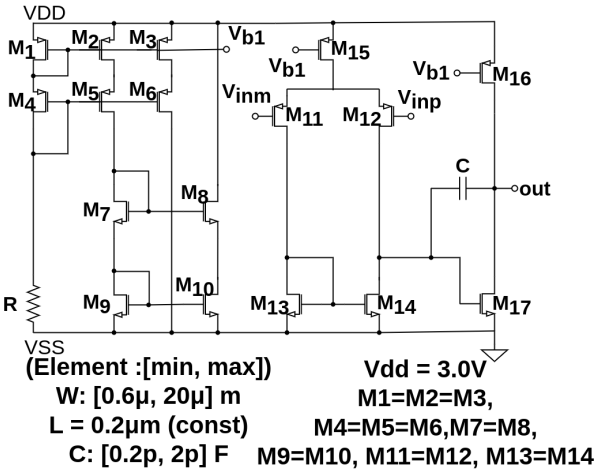

Fig. 2 criticPMOS differential pair and common source topology

loss function increases.

Next, we check the FoM for (1) and (2) and (3) and (4) shown in Fig. 4 and Fig. 5. The fact that the FoM of criticthe transferred model also increases with the number of simulations is only due to actor's critictraining.

In both cases, the increase in FoM in criticthe transferred model is larger than in training because the critic-training of critic has been completed, and the maximum FoM is higher than in training.

criticIn this experiment, we need to continue running simulation after the model critictransfer to calculate FoM, but most surprisingly, when we transfer the model, the simulation, which takes about 3 seconds per step, is not needed, saving roughly 480 seconds per topology sizing when random sampling is combined. This is not possible with DNN-Opt using FCNN, which cannot trasfer models.

4. Conclusion

These results indicate that DNN-Opt can transfer design

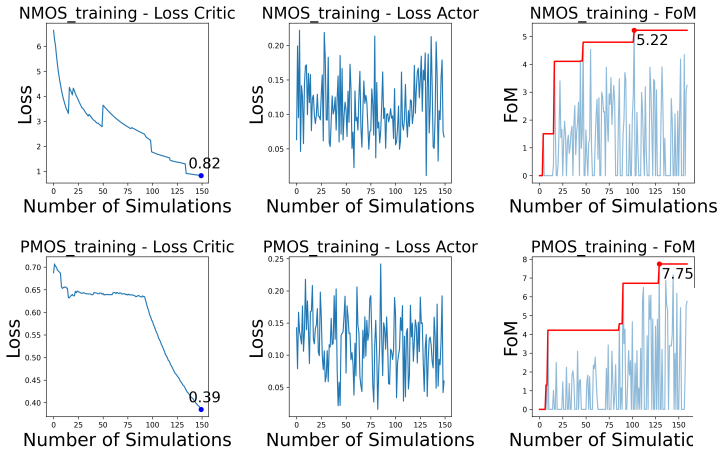

Fig. 3 lossfunction of GNN-Opt

knowledge between similar topologies, and that the increase in FoM is greater than training the model from criticscratch for the same number of simulations. There is still room for further modification of the GNN architecture and training methods to transfer models between more complex topologies. criticAfter criticmodel transfer, it obtains the FoM is equal to or better than a model trained from scratch without training critic, which means it doesn't need additional time-consuming simulations. criticWe think that this fact can be applied to a part of further high-speed sizing methods.

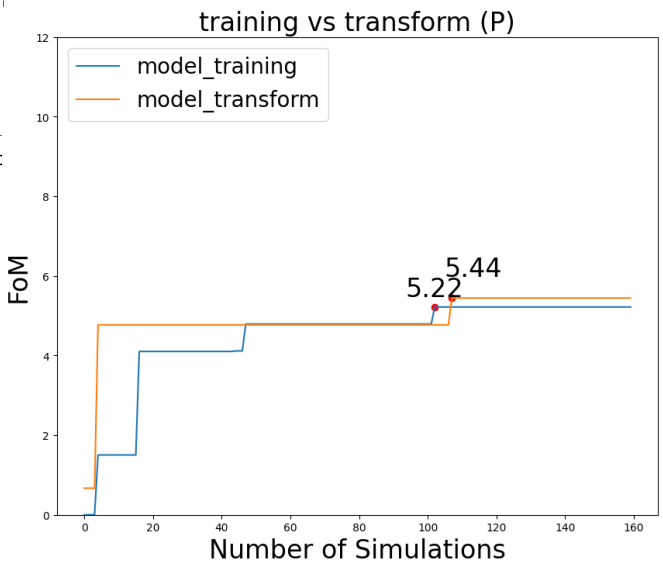

Fig. 4 FoM of NMOS differential

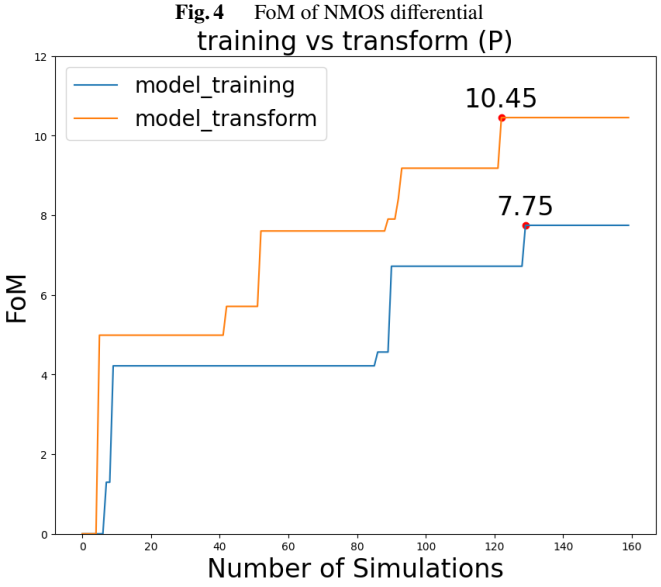

Fig. 5 FoM of PMOS differential

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