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PAPER Special Section on Analog Circuit Techniques and Related Topics

Continuous-Time Modeling of a Hysteretic DC-DC Converter using an Amplifier Model in place of the Hysteretic Comparator

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SUMMARY: This paper proposes the continuous-time modeling and analysis methods for a hysteretic buck DC–DC converter to examine its frequency characteristics (f-characteristics) and transient response. Determining the small-signal transfer function to derive the f-characteristics has been challenging due to the hysteretic behavior of the comparator. In this paper, the hysteretic comparator is modeled as an amplifier with a delay time between the input exceeding the hysteresis window boundary and the output state change, and with a voltage gain defined as the ratio between the comparator's output voltage change and the voltage difference of both input terminals during transition. The delay time is calculated based on the f-characteristics of the designed comparator circuits, and the voltage gain is determined using this delay time and the slew rate of the input signal. Subsequently, the overall small-signal transfer function and frequency characteristics are determined. It is also demonstrated that the proposed model accurately predicts the transient response when the load current changes. To verify the proposed modeling and analysis methods, a hysteretic buck DC–DC converter was designed and circuit-simulated using device parameters from a 0.18μm CMOS process. The simulation results closely matched the calculated frequency characteristics and the transient response.

key words: *Hysteretic comparator, Hysteretic buck DC–DC converter, Small-signal transfer function, Dynamic voltage gain, Delay time, Load current change*

1. Introduction

Switching DC-DC converters with hysteretic control are widely used in applications such as dynamic voltage scaling (DVS), wireless power transfer (WPT), sensor networks, mobile devices, CPUs, IoT microsensors [1]–[6], and DC–DC converter chips [7],[8]. In these applications, a fast and stable transient response at the output under sudden load voltage and current changes is essential. Low power consumption is also crucial for achieving high power efficiency [3],[5]. A switching DC–DC converter with hysteretic control is well-suited for achieving these objectives due to its simple control and compact circuitry.

However, no fully satisfactory models or equations currently exist to characterize the high-speed and/or low power capabilities of a hysteretic DC-DC converter. The challenge lies in deriving a small-signal transfer function, as the hysteretic comparator exhibits nonlinear characteristics.

In models for calculating the hysteretic DC-DC converters, the PWM switch model has been utilized [9],[10]. Reference 10 addresses hysteresis by adopting a control method where the inductor current is maintained within a hysteretic window, and its average values is fed back. However, this approach is not applicable to methods in which the comparator's terminal voltage exhibits hysteresis. Another approach involves using state equations, adding perturbations, and applying the Laplace transform to obtain the transfer function [1],[12]. While this method is more practical for circuit design, it also fails to model the hysteretic voltage comparator. The analysis and modeling of hysteretic converters have been discussed in [13]–[16]. The small-signal transfer function was derived considering a hysteretic voltage window in [14], however, the propagation delay of the hysteretic comparator was not fully accounted for in models [14]–[16].

Another method is discrete-time modeling, where the z-domain transfer function is used to model the comparator's operation, as the switch-mode controller functions similarly to a sampling amplifier [17],[18]. However, its applicability is limited to 50% duty cycle operation in [17]. Full modeling of hysteretic converters using advanced z-transforms was conducted in [18], where the f-characteristics of the entire converter were calculated. However, this approach does not take into account the f-characteristics of the comparator and requires highly complex calculations.

In contrast, we observed that the hysteretic comparator can be modeled as an amplifier with dynamic voltage gain and delay time, provided the amplifier's f-characteristics remain unchanged as the comparator's reference input voltage varies with hysteresis. In such cases, the continuous-time approach—utilizing state equations, perturbations, and the Laplace transform—becomes a viable option. However, the delay time was still determined through circuit simulation [19].

In this study, we present models developed using the continuous-time approach, along with a method to obtain the small-signal transfer function of the hysteretic comparator, based on actual circuit designs. We also provide a procedure to calculate the dynamic voltage gain and time delay. Furthermore, since none of the previous works addressed the transient response with load current changes using their modeling methods, we demonstrate that the comparator model in this paper successfully predicts this transient

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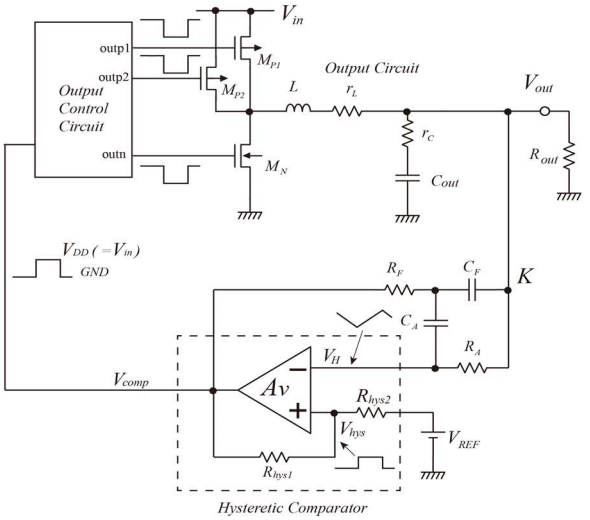


Fig. 1. Hysteretic buck DC–DC converter circuit.

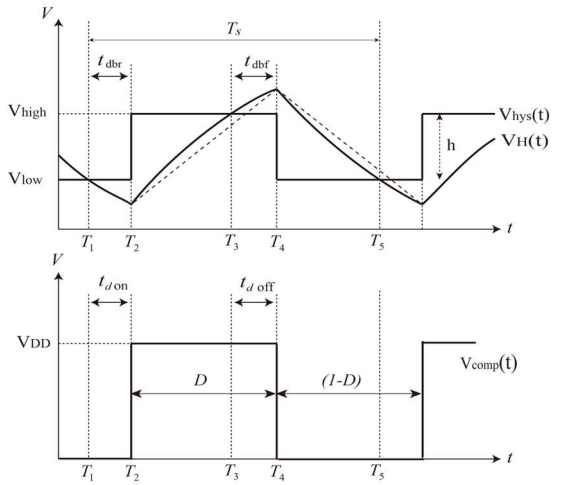


Fig. 2. Input & output waveforms of a hysteretic comparator.

behavior. To validate the proposed models and method, we compare the calculated frequency and transient characteristics obtained using MATLAB/Simulink™ with the SPICE circuit simulation results for a designed hysteretic buck DC-DC converter implemented in a 0.18 um CMOS process.

The paper is organized as follows: Section 2 introduces the hysteretic buck DC-DC converter circuit. In Section 3, we explain the principle of the modeling method for a hysteretic comparator. The small-signal transfer function is presented in Section 4, followed by the circuit design in Section 5. In Section 6, we compare the calculated frequency and transient response characteristics with the simulation results. Finally, Section 7 concludes the study.

2. Hysteretic Converter Circuit for the Modeling

Fig. 1 shows the circuitry of the hysteretic buck DC–DC converter employed in this modeling, analysis, and simulation to derive f-characteristics and the transient response. This converter operates on voltage feedback, and it requires a comparator with voltage hysteresis to be modeled. The hysteresis voltage is generated by feedback resistors R_{hys1} and R_{hys2}, while the comparator functions as a high-gain broadband amplifier. The voltage V_H at the inverting input terminal of the hysteretic comparator deviates repeatedly between the upper and lower limits of the hysteresis window. Consequently, V_H does not convey information regarding the inductor current. Control is executed in a manner ensuring that the average level of V_H (nearly V_{out}) aligns with the average level of V_{hys}. For switching power transistors, two PMOS transistors are prepared in parallel, along with one NMOS transistor.

3. Continuous-Time Modeling of the Hysteretic Comparator

The primary challenge lies in accurately modeling a hysteretic comparator. If it's feasible to model a hysteretic comparator using a linear amplifier, it might obviate the need for a discrete-time modeling approach. In Fig. 2, waveforms of V_H, V_{hys}, and V_{comp} are presented, representing the input voltage at the negative input terminal (denoted by the '–' sign), the voltage at the reference terminal (denoted by the '+' sign), and the output voltage of the hysteretic comparator in Fig. 1, respectively. Due to inherent delays within the comparator, the high state of V_{comp} shifts from time T_1 to T_2 and from T_3 to T_4 as shown in Fig. 2. The rising interval of V_H corresponds to the high state of V_{comp}, while the falling interval corresponds to the low state. Introducing the duty ratio D, which denotes the duration of V_{comp} when it remains high, reduces the control voltage V_{comp} to just two states: D and (1-D). Furthermore, if the amplifier f-characteristics remain consistent regardless of whether the voltage at the reference terminal is V_{high} or V_{low}, employing a common averaging method might suffice, rather than employing a discrete-time approach, as outlined in [18].

The key challenge lies in determining the time delays, t_{don} and t_{doff} in Fig. 2. Theoretically, V_{comp} changes its state at T_1 (T_3); however, practical considerations introduce delays, causing the change to occur at T_2 (T_4). When V_H increases, the hysteresis comparator functions as an amplifier with input voltages V_H at the negative terminal and V_{high} at the positive terminal. Conversely, as V_H decreases, the amplifier operates with V_H at the negative terminal and V_{low} at the positive terminal. If the frequency characteristics of the hysteretic comparator remain unaffected by changes in voltage at its positive terminal, comparisons can be conducted in a conventional manner, similar to those of a simple amplifier. Consequently, t_{don} and t_{doff} can be estimated using the amplifier's frequency characteristics.

In this study, the frequency characteristics of the amplifier, encompassing voltage gain and the –3 dB cutoff frequency, are

derived from circuit simulations of the designed circuits. This is essential because the time delays vary depending on the comparator circuit's configuration.

Fig. 3 shows the comparator circuit, which functions as an amplifier with differential inputs and a single-ended output, consisting of a two–stage amplifier. The inputs of the first amplifier are labeled 'inp' and 'inn,' with its output designated as 'out1'. A folded–cascode configuration is used to enhance the frequency characteristics. With a power supply of 3.6 V, the voltage at terminal 'out1' measures 2.9 V when the DC voltages at the input terminals 'inp' and 'inn' are equal. The second stage amplifier, shown in Fig. 3, incorporates transistors 'mpc09' and 'mnc10.' The voltage at terminal 'out1' is limited to a range of 2–3.6 V by a limiter transistor labeled 'nc04.' Fig. 4 presents a block representation of the comparator from Fig. 3, featuring a two-stage amplifier. Each stage comprises an ideal amplifier with a specific voltage gain and an R-C network representing first-order frequency characteristics.

The first stage amplifier exhibits a voltage gain A_{v1} of 40.7 dB (equivalent to 110 times amplification) and a –3 dB cutoff frequency f_{c1} of 7.94 MHz, as determined through SPICE circuit simulation. Following the change in state of V_{comp} in Fig. 2, the initial voltage difference at the input terminals of the first-stage amplifier approximately equals the hysteresis voltage h, which in this case is 0.1 V. Subsequently, the time t_{dh} taken for the voltages at both input terminals to become equal is given by the equation:

$$t_{dh} = h/a_{vh} \tag{1}$$

where a_{vh} represents the slew rate of the V_H signal.

When an initial input voltage difference of h is applied, the voltage at 'out1' terminal undergoes a change of hA_{v1}. As the input signal, characterized by a slew rate of a_{vh}, is fed into the amplifier with a voltage gain of A_{v1} and frequency response represented by $\omega_a/(s+\omega_a)$, where $\omega_a = 2\pi f_{c1}$, the voltage change hA_{v1} at the 'out1' terminal diminishes to zero after the delay time t_{da}. Consequently, the time t_{da} is determined as a solution to equation (2).

$$\mathcal{L}^{-1}\left\{\frac{a_{vh}}{s^2}\times\frac{A_{v1}\omega_a}{s+\omega_a}\right\}\Big|_{t=t_{da}} = \frac{a_{vh}A_{v1}}{\omega_a}(e^{-\omega_a t_{da}} + \omega_a t_{da} - 1) = hA_{v1} \tag{2}$$

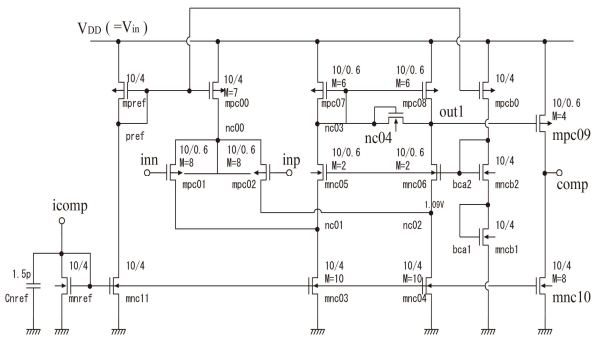


Fig. 3. Designed amplifier circuit used in the hysteretic comparator.

When the frequency and duty ratio of V_{comp} in Fig. 2 are set to 1.7 MHz and 50%, respectively, the slew rate a_{vh} is calculated to be $3.9e5\ V/\mu s$. This value of a_{vh} is determined by calculating the slope of the tangent of V_H at times T_1 and T_3. In equation (2), the exponential term $e^{-\omega_a t_{da}}$ is significantly smaller than $(\omega_a t_{da} - 1)$. Thus, t_{da} can be approximated as:

$$t_{da} \fallingdotseq \frac{h}{a_{vh}} + \frac{1}{\omega_a} \tag{3}$$

After calculating t_{dh} and t_{da} as $250\,ns$ and $270\,ns$, respectively, using equations (1) and (3), the delay time t_{d1} due to the frequency characteristics of the first-stage amplifier is determined as:

$$t_{d1} = t_{da} - t_{dh} = 20\,ns \tag{4}$$

This implies that the voltage at 'out1' is less than 2.9 V when the voltages of both input terminals are equal. The amount by which the voltage falls short of 2.9 V can be calculated as:

$$a_{vh}A_{v1}t_{d1} = (3.9e5) * 110 * (20e-9) = 0.843\,V \tag{5}$$

Hence, the 'out1' voltage at the time t_{dh} is estimated to be $2.9\,V - 0.843\,V = 2.057\,V$ (V_{out1L}) when the 'out1' terminal voltage increases. Conversely, when the 'out1' voltage decreases, the 'out1' terminal voltage is expected to be $2.9\,V + 0.843V = 3.743\,V$ (V_{out1H}). Although this voltage surpasses the supply voltage, no contradiction arises in the calculation.

The second-stage amplifier is characterized by a threshold voltage of 2.8 V (V_{in2}) within a supply voltage of 3.6 V. As previously demonstrated, the voltage at the 'out1' terminal becomes V_{out1L} when the voltages at both input terminals of the first-stage amplifier (i.e., the inputs of the hysteretic comparator) are equal. Consequently, the input voltage of the second-stage amplifier must transit from V_{out1L} to V_{in2} as the 'out1' terminal voltage increases, and from V_{out1H} to V_{in2} when it decreases. The slew rate at the input of the second-stage amplifier, namely the 'out1' terminal, is $a_{vh}A_{v1}$. Additionally, the second-stage amplifier possesses a gain A_{v2} of 76.5 dB (equivalent to 6,680 times amplification) and a –3 dB cutoff frequency f_b of 22.4 MHz. The time t_{dbf} required for the output voltage of the second-stage amplifier to change by $(V_{in2} - V_{out1L})A_{v2}$ is calculated in a manner similar to that described earlier.

$$\mathcal{L}^{-1}\left\{\frac{A_{v1}a_{vh}}{s^2}\times\frac{A_{v2}\omega_b}{s+\omega_b}\right\}\Big|_{t=t_{dbf}} = \frac{a_{vh}A_{v1}A_{v2}}{\omega_b}\left(e^{-\omega_b t_{dbf}} + \omega_b t_{dbf} - 1\right)$$

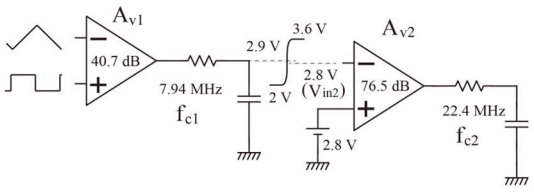


Fig. 4. Internal structure of the comparator in Fig. 3.

$$= (V_{in2} - V_{out1L})A_{v2} \quad (6)$$

where $\omega_b = 2\pi f_b$.

t_{dbf} is 24.7 ns. When the voltage of the 'out1' terminal decreases, the following formula is established, and the time t_{dbr} is calculated as:

$$\mathcal{L}^{-1}\left\{\frac{-A_{v1}a_{vh}}{s^2} \times \frac{A_{v2}\omega_b}{s+\omega_b}\right\}\Big|_{t=t_{dbr}} = (V_{out1H} - V_{in2})A_{v2} \quad (7)$$

t_{dbr} becomes 29.5 ns. Thus, in general, the delay time of the comparator in operation can be calculated by knowing a slew-rate of an input signal and frequency characteristics of the designed circuit.

Now, these t_{dbf} and t_{dbr} values are utilized to determine the dynamic voltage gain of the comparator. As shown in [19], the dynamic voltage gain is calculated by taking the ratio between the output voltage change (V_{cc} in this case) and the input voltage change of the comparator precisely before the transition occurs. The dynamic voltage gains at times T2 and T4 differ, and they are averaged to obtain the average gain A_{teq} for one cycle period by calculating the weighted sum using the duty factor D:

$$A_{teq} = \frac{D \times V_{DD}}{\dot{V_H}(T_1) \times t_{dbr}} - \frac{(1-D) \times V_{DD}}{\dot{V_H}(T_3) \times t_{dbf}} \quad (8)$$

Here, $\dot{V_H}(T_x)$ represents the derivative of V_H at time T_x, where x is 1 or 3. The voltage difference between the inputs of the comparator at the transition is approximated by $\dot{V_H}(T_x) \times t_{dby}$, where y denotes r or f, assuming that the V_H curve changes linearly during this short time interval.

Here, the V_H curve is determined by the external components R_F and C_F in Fig. 1, provided that $Z_{C_F} < Z_{C_A} + Z_{R_A}$, where Z represents the impedance [18]. When V_{comp} increases, the voltage between both ends of the C_F capacitor increases as follows:

$$v_{CFR}(t) = \left(V_{compH} - V_{out} - V_{cf0}\right)\left(1 - e^{-\frac{1}{R_F C_F}t}\right) + V_{cf0} \quad (9)$$

where V_{compH} is the voltage of the comparator output in the high state (V_{cc} in this case) and V_{cf0} is the initial voltage difference between both ends of the C_F immediately before V_{comp} becomes high at T_2 in Fig. 2. $V_H(t)$ increases by approximately h at T_4. When V_{comp} becomes low, the voltage between both ends of the C_F decreases as follows:

$$v_{CFF}(t) = \left(V_{cf0} + h - V_{compL} + V_{out}\right)e^{-\frac{1}{R_F C_F}t} + \left(V_{compL} - V_{out}\right) \quad (10)$$

The rising time interval t_r of $V_H(t)$ is calculated as the time at which $V_H(t)$ crosses $V_{cf0} + h$ line by equating $v_{CFR}(t)$ to $V_{cf0} + h$ in (9), and the falling time interval t_f when $V_H(t)$ crosses V_{cf0} line by equating $v_{CFF}(t)$ to V_{cf0}. The differentiations of $V_H(t)$ at time T_3 and T_1 are,

$$\dot{V_H}(T_3) = -\frac{1}{R_F C_F}\left(-V_{compH} + V_{out} + V_{cf0}\right)e^{-\frac{1}{R_F C_F}t_r} \quad (11)$$

$$\dot{V_H}(T_1) = -\frac{1}{R_F C_F}\left(V_{cf0} + h - V_{compL} + V_{out}\right)e^{-\frac{1}{R_F C_F}t_f} \quad (12)$$

Because V_{compH} and V_{compL} is approximately equal to V_{cc} and zero, respectively, the A_{teq} of the hysteresis comparator can be derived.

4. Small-Signal Transfer Function of a Hysteretic Buck DC-DC Converter

The small-signal transfer function of the hysteretic comparator is formed by connecting the dynamic transition gain A_{teq} in series with its input-to-output delay e^{-st_D}, accounting for the slew rate of the input signal. Here, t_D represents the average of t_{dbr} and t_{dbf}. Fig. 5 illustrates the blocks in the form of those used in MATLAB/Simulink™, with each block representing the small-signal transfer function corresponding to a circuit within the entire buck DC–DC convertor shown in Fig. 1. $G_{LCR}(s)$ and $Z_{CR}(s)$ in series represent the transfer function of the output circuit. The on-state resistances of power switch transistors M_n and M_ps are taken into account as R_n and R_p, respectively. $G_1(s)$ represents the small-signal transfer function from the output of the hysteretic comparator to its inverting node, while $G_2(s)$ denotes the transfer function from the output of the entire buck DC–DC converter to the inverting node of the hysteretic comparator.

Table 1 lists the transfer function of each block in Fig. 5, except for the delay blocks $e^{-st_{dL}}$ and e^{-st_D}. The dynamic gain of the comparator, A_{teq}, is calculated using Equation (8).

The values of $\dot{V_H}(T_1)$ and $\dot{V_H}(T_3)$ are calculated using Equations (11) and (12), and these correspond to VhT1 and VhT3 in Table 1, respectively. The delay $e^{-st_{dL}}$ represents the logic delay of the output control circuit shown in Fig. 1.

The open-loop small-signal transfer function $T_{all}(s)$ of the hysteretic buck DC–DC converter is now calculated. The line indicated by K is cut, and the input signal v_{in} is applied to the block $G_2(s)$ in Fig. 5. It becomes:

$$T_{all}(s) = \frac{\Delta v_{out}(s)}{\Delta v_{in}(s)} = \frac{G_2 C e^{-st_D}}{1 - G_1 C e^{-st_D}} \times \frac{1}{V_{DD}} e^{-st_{dL}} G_{LCR} Z_{CR} \quad (13)$$

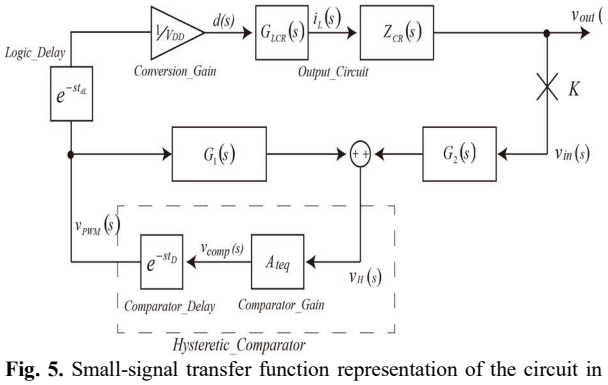


Fig. 5. Small-signal transfer function representation of the circuit in Fig. 1.

Table 1 Small-signal transfer function of each block shown in Fig. 5.

$G_{LCR}(s) = \dfrac{[C_{out}(R_{out}+r_C)\{V_{out}(R_n-R_p)+V_{in}R_{out}\}]s + V_{out}(R_n-R_p)+V_{in}R_{out}}{\{LR_{out}C_{out}(R_{out}+r_C)\}s^2 + [LR_{out}+R_{out}C_{out}(R_{out}+r_C)\{-D(R_n-R_p)+R_n+r_L\}+C_{out}r_C{R_{out}}^2]s + (R_n+r_L)R_{out}-D(R_n-R_p)R_{out}+{R_{out}}^2}$
$Z_{CR}(s) = \dfrac{(R_{out}C_{out}r_C)s+R_{out}}{C_{out}(R_{out}+r_C)s+1}$
$G_1(s) = \dfrac{(R_AC_A)s}{(R_AR_FC_AC_F)s^2+\{R_F(C_F+C_A)+R_AC_A\}s+1}$
$G_2(s) = \dfrac{(R_AR_FC_AC_F)s^2+(R_FC_F+R_FC_A)s+1}{(R_AR_FC_AC_F)s^2+\{R_F(C_F+C_A)+R_AC_A\}s+1}$
$A_{teq} = \dfrac{DV_{DD}}{(t_{dbr}\times VhT1)} - \dfrac{(1-D)V_{DD}}{(t_{dbf}\times VhT3)}$

When considering models for transients, the voltage changes at various nodes must be accounted for in both the comparator block and the output block. The output circuit should also be represented using a state equation. Fig. 6 shows the blocks modeled using MATLAB/Simulink™ for transient analysis during load current changes.

Essentially, the same amplifier parameters—such as amplifier gain and time delay—along with the same feedback functions G1 and G2, are presented in Fig. 6. The main differences from Fig. 5 are the hysteresis voltage generation in the comparator section and the state equation representation in the output part of the converter. The dump control signal block provides a signal to change the output resistor R_{out} in Fig. 1.

One major difference between our approach and that in reference [18] is that our method allows precise modeling of transients, such as load current changes, whereas the method in reference [18] does not. Another key difference is that our continuous-time model considers the amplifier's voltage gain and the time delay during operation in a hysteresis comparator, accounting for the slew rate at its input. In contrast, the comparator in reference [18] is characterized by the ratio $\Delta d/\Delta V_{REF}$, as found in equation (20) of the reference, where Δd represents the variation in the duty cycle and ΔV_{REF} represents the variation in reference voltage. This ratio is determined solely by the slope of V_H, which depends only on the values of D, R_F and C_F, without considering the role of the amplifier.

5. Circuit Design for the Hysteretic buck DC-DC converter

To validate our modeling approach for the hysteretic comparator, which closely aligns with the actual circuit, we implemented hysteretic buck DC–DC converter circuits using device parameters from a 0.18 μm CMOS process. Frequency and load current variations were then simulated using SPICE.

Fig. 7 illustrates the circuit used for the transient simulation in SPICE. The circuits of the 'Buff_in' block, the 'erramp' block within the hysteresis amplifier, and the output power transistors were designed using the 0.18um CMOS process.

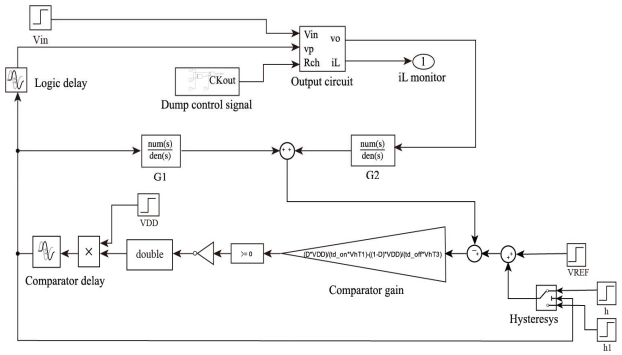


Fig. 6. Block representation for the transient analysis.

5.1 Hysteretic comparator circuit

The designed comparator circuit is shown in Fig. 3. The hysteresis voltage is determined by external resistors. The comparator consists of two-stage amplifiers, with the output voltage of the first amplifier at the 'out1' terminal constrained by the 'nc04' transistor to ensure symmetrical positive and negative voltage swings. As a result, the delay is calculated in two stages.

The triangular waveform V_H at the inverting input terminal 'inn' of the 'erramp' is primarily generated using resistor R_F and capacitor C_F, given the duty factor D, as shown in Fig. 1. The hysteresis voltage of the comparator is set to approximately 100 mV, established by connecting external resistors R_{hys1} and R_{hys2}.

The component values for $R_F, C_F, R_A,$ and C_A are determined as follows. As indicated in equations (9) and (10), the time constants must satisfy the relationship $R_FC_F < R_AC_A$. The waveform V_H in Fig. 2 is primarily determined by R_FC_F. During the design process, D is set to 0.5 of the time interval T_S, so in this case, $V_{out} = DV_{CC}$.

In the ideal case, both $v_{CFR}(DT_S)$ in equation (9) and $v_{CFF}((1-D)T_S)$ in equation (10) are equal to the hysteresis voltage $V_{hys} = h$. Based on this, the values of R_F and C_F are determined. R_A and C_A are then selected to maintain the aforementioned relationship.

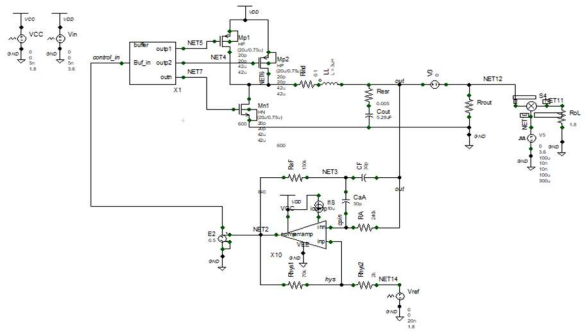


Fig. 7. The SPICE transient simulation circuit based on the use of the designed circuit.

5.2 Output control and output circuits

The output switching transistors consist of two PMOS power transistors, M_{p1} and M_{p2}, and one NMOS transistor, M_N, as shown in Fig. 1. Each PMOS transistor has a gate width of 12,000 μm and a gate length of 0.75 μm. The NMOS transistor has a gate width of 16,800 μm, also with a gate length of 0.75 μm. The on-resistance of the PMOS transistors, estimated for the parallel connection of M_{p1} and M_{p2}, is 0.2 Ω, while for M_N, it is 0.1 Ω. A series resistance r_L of 0.1 Ω is selected for the inductor L, and an equivalent series resistance (ESR) r_c of 5 mΩ is assigned to the capacitor C_{out}.

The buffer circuit has three output terminals: two for the PMOS transistors and one for the NMOS transistor. It is designed using a 0.18μm CMOS process. To prevent waveform overlap, the driving signals for both the PMOS and NMOS transistors are adjusted with a time delay. This delay is generated using a CMOS switch configuration along with a stray capacitor.

6. Simulation Results and Comparative Analysis

For comparison purposes, SPICE circuit simulations were performed using the practically implemented circuits. To simulate the open-loop frequency characteristics in SPICE, a 50 Ω resistor was introduced between V_{out} and point K in Fig. 1, following a line cut. The input signal was then applied across the 50 Ω resistor, and the amplitude and phase at the V_{out} terminal were recorded.

In this study, four types of simulations were conducted. Three simulations involved different output voltages, while the fourth examined the transient response when the load current changed. The parameters V_{in}, V_{DD}, L, r_L, C_{out}, r_c, and h were fixed at 3.6 V, 3.6 V, 3 μH, 0.1 Ω, 5.28 μF, 5 mΩ, and 0.1 V, respectively, for all simulations. The values of the feedback elements R_F, C_F, R_A, and C_A were set 150 KΩ, 30 pF, 240 KΩ, and 30 pF, respectively, so that the ideal clock frequency was 2 MHz. Other elements used in the simulations are listed in Table 2.

However, the calculated clock frequencies are ideal values. Due to the time delay in the comparator, the V_H signal surpasses the hysteresis limit h, resulting in lower actual clock frequencies. Although the ideal hysteresis voltage h was set to 0.1 V, it was increased by about 20 % to account for the comparator's time delay in the calculations. The delays t_{dbf} and t_{dbr} were calculated using equations (6) and (7), respectively.

To assess the impact of voltage gain and time delay variation of a hysteretic comparator on the frequency characteristics of an entire hysteretic buck DC–DC converter, we applied the transfer function in (13) to plot the Bode diagram of the converter. Fig. 8 illustrates the difference in the three t_Ds. All parameters and element values were identical to those of the 2 M_typ in Table 2. The delay time t_D of 27.1 ns in the 2M_typ case was the mean of t_{dbf} and t_{dbr} calculated using equations (6) and (7), respectively. The other two t_D values were chosen to be half and double the typical delay time.

The dynamic voltage gain of a hysteretic comparator is strongly dependent on the delay time t_D, as defined by equation (8). As shown in Fig. 8, variations in the open-loop gain and phase at low frequencies were observed. The changes at higher frequencies were primarily due to variations in the delay time. Therefore, deviations in frequency characteristics occur if the delay time estimation is inaccurate.

Subsequently, four different SPICE simulations were performed with an ideal clock frequency of 2 MHz, again utilizing the parameters listed in Table 2. The actual clock frequency becomes less than 2 MHz.

Fig. 9 presents three Bode plots, illustrating the ideal clock setting at 2 MHz. Figures 9(a), 9(b), and 9(c) show scenarios with V_{out} at 2.7 V and an ideal duty factor D of 0.75; V_{out} at 1.8 V and an ideal duty factor D of 0.5; and V_{out} at 0.9 V and an ideal duty factor D of 0.25, respectively. The load current remains constant at 0.3 A across all cases, while the frequency range spans from 10 Hz to 3 MHz. Bold lines represent $T_{all}(s)$, as defined in equation (13), while crosses—ranging from 100 Hz to 200 kHz or 400 kHz— depict the SPICE simulation results.

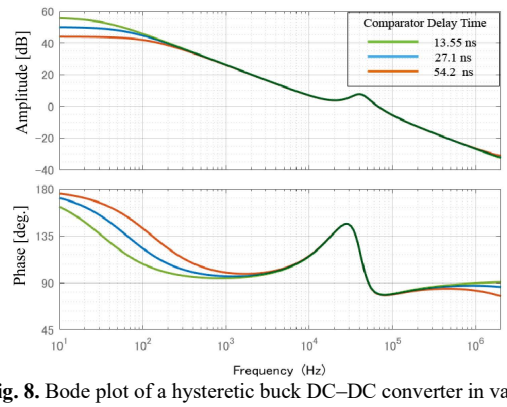


Fig. 8. Bode plot of a hysteretic buck DC–DC converter in varying delay of a hysteretic comparator. (Ideal fsw is 2M_typ in table 2.)

Table 2 Device parameters for circuit simulations.

Ideal fSW (Actual) [Hz]	Transient 2M_typ	2M_low	2M_typ (1.67M)	2M_high
V out [V]	1.8	0.9	1.8	2.7
V REF [V]	1.8	0.9	1.8	2.7
R out [Ω]	60 ⟷ 1.8	3	6	9
D	0.5	0.25	0.5	0.75
td_on (t dbr) [s]	29.5n	31.7n	29.5n	28.7n
td_off (t dbf) [s]	24.7n	25.5n	24.7n	22.5n

Despite variations in output resistance R_{out}, these alterations in V_{out} do not significantly affect the small-signal transfer function, resulting in similar characteristics across all three cases. While a 2 to 3 dB difference in gain peaks is apparent in all cases, overall, both the calculated and SPICE frequency characteristics are in close agreement.

Fig. 10 shows a comparison between the SPICE-generated and MATLAB/Simulink™-generated transient waveforms at V_{out} when the load current switches between 30 mA and 1030 mA. The ideal clock frequency is set to 2 MHz, with a duty cycle D of 0.5, resulting in V_{out} being 1.8 V. The supply voltage V_{CC} is applied at time zero. The SPICE circuit used is the same as the one shown in Fig. 7. The operation proceeds as follows: initially, the output resistor R_{rout} is 60 Ω, resulting in an average inductor current of 30 mA. At 100 µs, an additional output resistor R_{OL}, with a value of 1.8 Ω is activated in parallel with R_{rout}, causing the inductor current to rise to 1030 mA. Then, at 200 µs, R_{OL} is removed, and the inductor current returns to 30 mA. The output terminal voltage V_{out} deviates in response to changes in the inductor current.

In Fig. 10, the curve marked as the 'red line' represents the SPICE simulation result, while the curve marked as the 'black line' corresponds to the MATLAB/Simulink™ simulation result on the block diagram shown in Fig. 6. It is evident that both red (SPICE) and black (our model) lines coincide at 100 µs and 200 µs, as well as during the startup interval.

Another concern is whether our models can be applied to DCM operation. In Fig. 10, changes in the inductor current

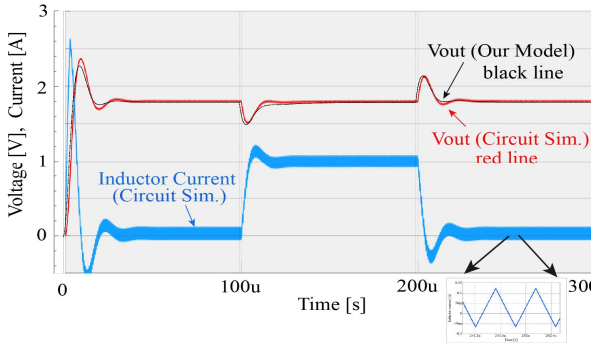
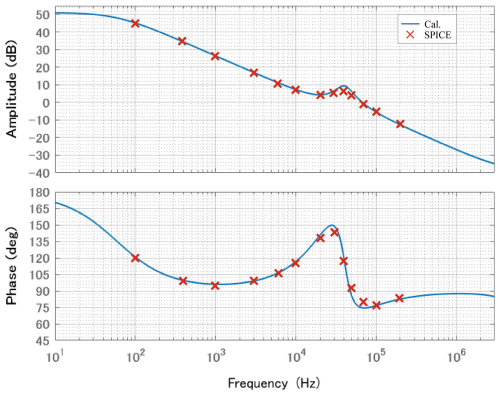
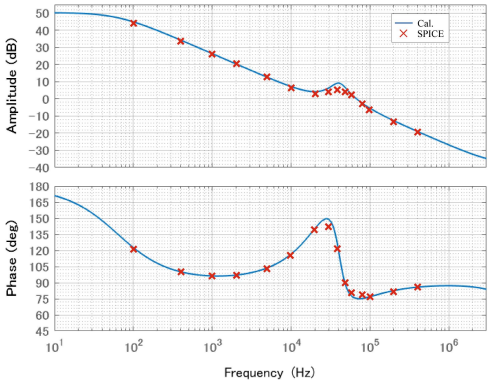


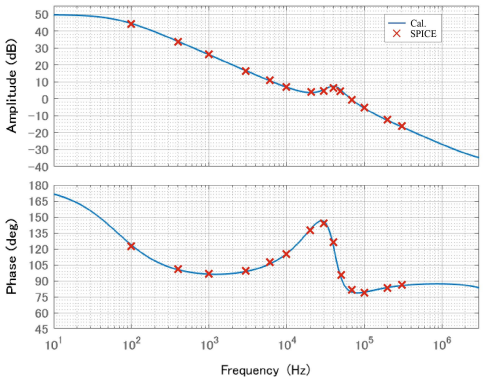
Fig. 10. Comparison of the transient at the output with the load current change, and the waveform of the inductor current.



(a) $V_{out} = 2.7\ V, R_{out} = 9\ \Omega,\ f_{sw} = 1.23\ MHz$



(b) $V_{out} = 1.8\ V, R_{out} = 6\ \Omega,\ f_{sw} = 1.67\ MHz$



(c) $V_{out} = 0.9\ V, R_{out} = 3\ \Omega,\ f_{sw} = 1.43\ MHz$

Fig. 9. Bode plot. Ideally 2 MHz setting for the switching frequency.

are shown, with an enlarged portion of the waveform displayed. The inductor current of 30 mA indicates that the current crosses the 0 A line during one clock interval. However, the inductor current waveform remains continuous and does not stay zero, even when it touches the 0 A line. This is because neither the circuit in Fig. 1 nor the block diagram in Fig. 6 includes functionality to analyze DCM operation. Therefore, the modeling method presented in this paper should be limited to CCM operation. Nonetheless, we believe our model could be adopted to correspond to DCM operation in the future [20].

7. Conclusion

We propose a continuous-time modeling approach for a hysteretic DC–DC converter that closely aligns with the actual circuit. In this approach, the non-linear hysteretic comparator is replaced by the voltage gain and time delay of a linear amplifier at the operating speed, accounting for the input's slew rate. This eliminates the need for a complex discrete-time state-space approach. The proposed model has been validated by comparing its frequency characteristics and transient response with results from SPICE simulations of the actual designed circuit. The agreement between them demonstrates the effectiveness of the proposed continuous-time modeling method.

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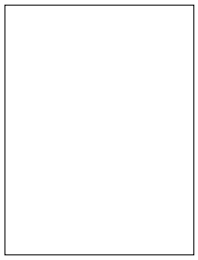

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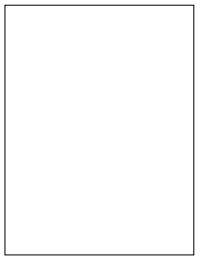

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