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PAPER Special Section on Analog Circuit Techniques and Related Topics

A Load Voltage Estimation and Regulation System for Wireless Power Transfer with Optimum Matching Circuit Design

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SUMMARY A load voltage estimation and regulation system for wireless power transfer circuits exploiting only primary-side control is proposed. The proposed system provides regulated load voltage independent of load and coupling conditions, using neither a secondary-side controller nor an external coil for intercommunication, as required in conventional systems. Adaptive frequency control based on a phase-locked loop technique enables the estimation of load voltage using only the electric parameters measurable on the primary side. Some formulas for voltage estimation and for designing a two-port matching circuit on the secondary side to maximize power transfer efficiency are derived. The versatile and explicit design formulas allow designers to easily determine circuit parameters to theoretically maximize efficiency corresponding to the specifications of each application. It is confirmed that a prototype system implemented on an one-coin-sized printed circuit board regulates the load voltage for several values of load and coupling coefficient.

key words: *wireless power transfer, load voltage regulation, voltage estimation, phase-locked loop, power transfer efficiency, two-port circuit*

1. Introduction

Wireless power transfer (WPT) technologies play an important role in biomedical implantable devices (BIs) such as cochlear implants [1], [2] or visual prostheses [3], [4]. In case a battery is placed on human skin for ease of replacement and cables penetrating the skin cannot be used for hygiene reasons, WPT is the only one solution to deliver power to BIs. Several types of method for realizing WPT have been studied such as utilizing microwaves [5] or lasers [6]. For BIs, magnetic coupling between transfer coils is typically utilized for power transfer [7].

One of the issue of a WPT system exploiting magnetic coupling is the load voltage fluctuation caused by variations of a load and a coupling coefficient. The former is ascribable to a dynamic changes in the dissipated power of BIs. Especially, in case the operation mode of BIs is adaptively selected, such as in sleep mode or active mode, the variation in the dissipated power becomes relatively large. The latter is due to the individual variation of the thickness of human skin. Since load voltage fluctuations may cause malfunctions of BIs, a voltage regulation is needed.

Since the power dissipation of regulation circuitry should be low as much as possible to extend battery life and to reduce heat, a linear regulator is unsuitable for BIs. A switching voltage converter is one of the candidates thanks to its high efficiency, although it comes with a higher cost and increases system volume. As another candidate for voltage regulation, a regulated rectifier, which realize both functionalities of rectification and voltage regulation with one chip, have been widely studied [8]–[11]. Although several types of regulated rectifiers have been proposed, a fundamental concept is roughly common. The load voltage regulation is achieved by switching the configuration of a rectifier using active switches. For example, since a full-wave rectifier can transfer more energy from its input to a load compared to a half-wave rectifier, selecting whether to use a half- or a full-wave rectifier with load voltage sensing results in the voltage regulation. A problem of this regulation method is the degradation of overall system efficiency especially at light-load conditions. This is because an AC power amplifier (PA) on a primary side supplies excessive power regardless of load conditions. To overcome the problem, the regulation systems with both primary- and secondary- side control have been proposed [12]–[16]. A regulated rectifier on a secondary side finely regulates load voltage while a primary-side controller adjusts the output power of a PA depending on load conditions, which is sensed with a load shift keying (LSK) technique. This control makes overall efficiency better thanks to the adaptive power control, however, an external sensing coil at the cost of size is needed to sense the load conditions on a primary side. Recently the both-side control method without any of sensing coils is reported [17], while it suffers from the power dissipation of the circuit for LSK.

If load voltage is known on a primary side, voltage regulation is achieved only with primary-side control. It is expected that primary-side-only control improves overall efficiency thanks to eliminating the power losses of a secondary-side controller. It is desired that load voltage is known on a primary side without any of external communication circuitry since it wastes power and increases system complexity. Therefore to estimate load voltage on a primary side without any of feedback communications is key point to realize the control. Some contrivance should be needed to estimate load voltage since a WPT circuit includes two unknown parameters that cannot be measured on a primary side: a load and a coupling coefficient. Reference [18] proposed a voltage estimation and regulation method exploiting an adaptive frequency control with a particular secandory-side circuit configuration. However, the reference did not

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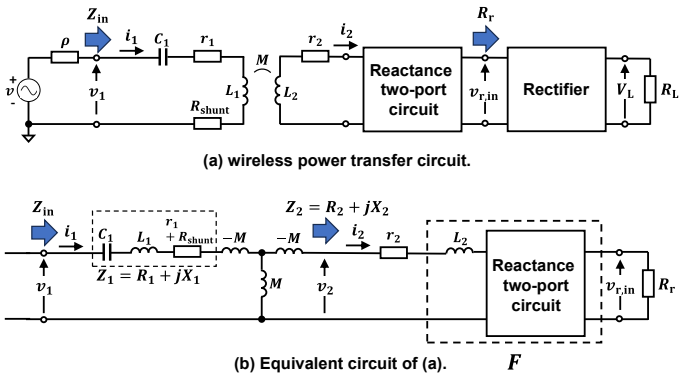

Fig. 1 Wireless power transfer circuit structure.

consider the circuit configuration to increase power transfer efficiency. Moreover, the operation of a proposed voltage regulation controller is confirmed just only simulation with some ideal circuit components.

This paper proposes and implements a load voltage regulation system only with primary-side control. The estimation method proposed in Ref. [18] is generalized to arbitrary secondary-side circuit configurations. Design formulas and examples of the secondary-side circuit to maximize system efficiency are provided. The prototype system implemented on an one-coin size printed circuit board validates the effectiveness of the proposed method.

2. Load voltage estimation using electrical parameters measured on primary side

2.1 Estimation utilizing zero-reactance condition

Figure 1(a) shows the WPT circuit analyzed in this paper. The sinusoidal voltage source whose open voltage, the output resistance, and the angular frequency are v, ρ and ω, respectively, supplies the input current i_1. The capacitor for resonance C_1 is connected in series with the transmission inductor L_1. On the secondary side, the two-port reactance circuit to realize desired circuit characteristics and the rectifier are connected between the inductor L_2 and the load R_L. The n-th side inductor $L_n (n = 1, 2)$ are magnetically coupled with mutual inductance $M = k\sqrt{L_1 L_2}$ where k denotes a coupling coefficient. r_n represents the equivalent series resistance (ESR) of L_n, and R_shunt does the small shunt resistance connected in series for current measurement.

Our aim is to regulate the load voltage V_L to be the desired reference voltage V_REF regardless of changes in the varied parameters R_L and k only with primary-side control. The values of the varied parameters should be known on the primary side to know V_L while they cannot be measured directly. The proposed load voltage regulation consists of 4 steps for estimating the varied parameters using only the electrical parameters measurable on the primary side. Here we explain how to estimate the equivalent input resistance of the rectifier R_r because it is used to estimate R_L and V_L in following steps. It is assumed that the circuit parameters except for R_L and k are known in advance.

First, the overall input impedance $Z_\mathrm{in} \stackrel{\mathrm{def}}{=} v_1/i_1$ is analyzed because it is an important parameter for the estimation. Figure 1 (b), which is the equivalent circuit of Fig 1 (a), is utilized for the analysis. Noting that the input impedance of the T-shaped circuit consists of the inductors $-M$ and M is inversely proportional to the load impedance Z_2,

$$Z_\mathrm{in} = Z_1 + \frac{(\omega M)^2}{Z_2} \tag{1}$$

is satisfied, where Z_1 denotes the impedance of the series resonance circuit on the primary side and Z_2 does the input impedance of the secondary side. By defining Z_n as $R_n + jX_n$, $R_1 = r_1 + R_\mathrm{shunt}$ and $X_1 = \omega L_1 - 1/(\omega C_1)$ holds. On the secondary side, expressing the reactance two-port circuit including L_2 with the chain matrix notation

$$\boldsymbol{F} \stackrel{\mathrm{def}}{=} \begin{pmatrix} A & jB \\ jC & D \end{pmatrix} \tag{2}$$

gives the expression for R_2 and X_2 as

$$R_2 = r_2 + \mathrm{Re}\left[\frac{A + j\dfrac{B}{R_\mathrm{r}}}{jC + \dfrac{D}{R_\mathrm{r}}}\right] = r_2 + \frac{R_\mathrm{r}}{(CR_\mathrm{r})^2 + D^2}, \tag{3}$$

and

$$X_2 = \mathrm{Im}\left[\frac{A + j\dfrac{B}{R_\mathrm{r}}}{jC + \dfrac{D}{R_\mathrm{r}}}\right] = \frac{BD - ACR_\mathrm{r}^2}{(CR_\mathrm{r})^2 + D^2}. \tag{4}$$

It is noted that diagonal elements and non-diagonal elements of the chain matrix of a reactance network are purely real and imaginary, respectively [19], parameters A, B, C and D are all real numbers. Decomposing the right-hand side of Eq. (1) into its real and imaginary parts yields

$$Z_\mathrm{in} = R_1 + \left(\frac{\omega M}{|Z_2|}\right)^2 R_2 + j\left(X_1 - \left(\frac{\omega M}{|Z_2|}\right)^2 X_2\right). \tag{5}$$

The right-hand side of the above equation includes two unknown parameters M and R_r since R_2 depends on R_r. The values of the unknown parameters are known by solving the nonlinear simultaneous equation that is obtained by substituting the measured values of the phase and the magnitude of Z_in into the left-hand side. However, solving a simultaneous nonlinear equation requires a numerical method that may take a long time to converge or may diverge with inappropriate initial values. Therefore it is desirable that the unknown parameters can be calculated with an analytical process.

An analytical parameters derivation is realized by adjusting the driving frequency to meet the zero-reactance condition

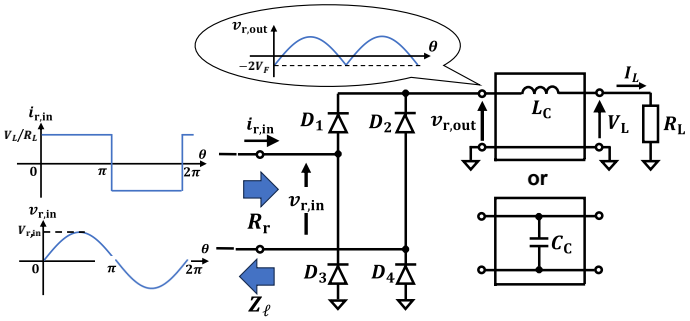

Fig. 2 Bridge rectifier and waveforms of one driven by sinusoidal input voltage $v_{r,in}$.

$$\mathrm{Im}[Z_{in}] = 0 \leftrightarrow \left(\frac{\omega_{ZR} M}{|Z_2|}\right)^2 = \frac{X_1}{X_2}, \tag{6}$$

where ω_{ZR} represents the angular frequency at which the input reactance $\mathrm{Im}[Z_{in}]$ becomes 0. Although ω_{ZR} depends on the varied parameters M and R_r, it can be automatically tracked using a phase-locked loop (PLL) technique [20], [21]. Substituting Eq. (6) into Eq. (5) yields

$$R_{in,ZR} = R_1 + R_2 \frac{X_1}{X_2} \tag{7}$$

where $R_{in,ZR}$ denotes the input resistance at ω_{ZR}. It is worth noting that one of the unknown parameter M is eliminated thanks to the frequency tuning.

Next, the left unknown parameter R_r is estimated as one of solutions of Eq. (7). From Eqs. (3) and (4), only R_2 and X_2 are variables containing the unknown parameter R_r. Separating the known- and unknown- parameters on Eq. (7) leads to

$$\frac{X_2}{R_2} = \frac{X_1}{R_{in,ZR} - R_1} \left(\stackrel{\mathrm{def}}{=} \alpha\right). \tag{8}$$

Let the right-hand side be α, whose value is known on the primary side by measuring ω_{ZR} and $R_{in,ZR}$, simplifying Eq. (8) as

$$\frac{X_2}{R_2} = \alpha. \tag{9}$$

Substituting Eqs. (3) and (4) into the above equation yields

$$\frac{BD - ACR_r^2}{r_2[(CR_r)^2 + D^2] + R_r} = \alpha, \tag{10}$$

which is the quadratic equation for R_r. Its solution for R_r gives a formula of the estimated load

$$R_{r,est} = \frac{-\alpha \pm \sqrt{\alpha^2 - 4CD(\alpha r_2 C + A)(\alpha r_2 D - B)}}{2C(\alpha r_2 C + A)}. \tag{11}$$

Substituting the measured values of α and ω_{ZR} into this formula gives the estimated load value $R_{r,est}$. Note that the plus-minus sign in Eq. (11) gives two candidates for the estimated load, one of which is correct and the other is incorrect. However, with the two-port network designed later, a correct estimated value is distinguished because one of the estimated value becomes negative, which is obviously inappropriate from a physical point of view.

As the third step, the amplitude $V_{r,in}$ of the rectifier input voltage $v_{r,in}$ is estimated since it is necessary to know the load voltage V_L. Note that we hereafter use a lowercase letter to denote an AC voltage or current and does a uppercase letter to denote a DC voltage or current or an amplitude of an AC one. $V_{r,in}$ is easily known on the primary side thanks to the frequency tuning. At $\omega = \omega_{ZR}$, the power balance leads to

$$I_1^2 R_{in,ZR} = I_1^2 r_1 + I_2^2 R_2 \tag{12}$$

$$I_2 = I_1 \sqrt{\frac{R_{in,ZR} - r_1}{R_2}} \tag{13}$$

where $I_n (n = 1, 2)$ represents the amplitude of i_n. The right-hand side of the equation does not have one of the unknown parameter M. Since the transfer ratio from $V_{r,in}$ to I_2 is given by

$$\frac{V_{r,in}}{I_2} = \frac{1}{\sqrt{C^2 + \left(\frac{D}{R_r}\right)^2}} = \frac{R_r}{\sqrt{(CR_r)^2 + D^2}}, \tag{14}$$

substituting Eq. (13) into Eq. (14) yields

$$V_{r,in} = I_1 R_r \sqrt{\frac{R_{in,ZR} - r_1}{R_2} \frac{1}{(CR_r)^2 + D^2}}. \tag{15}$$

$V_{r,in}$ is known by substituting the measured values of $I_1, R_{in,ZR}$ and the estimated load obtained with Eq. (11) into this equation.

2.2 load voltage estimation

As the final step, we examine the characteristics of a rectifier to clarify the relationship between the amplitude $V_{r,in}$ of the input voltage $v_{r,in}$ and the load voltage V_L. Figure 2 shows a bridge rectifier with two types of smoothing element: a choke inductor L_c or a large capacitor C_c. For simple analysis, we assume that the waveforms of the input voltage $v_{r,in}$ or current $i_{r,in}$ are sinusoidal. The former assumption gives accurate approximation when the magnitude of the impedance looking left from the rectifier's input terminal $|Z_\ell|$ is relatively smaller than R_r. This is because the Thevenin equivalent circuit of a circuit connected forward to the rectifier is an voltage source the output impedance of which is very smaller than that of its load and can be considered as an ideal voltage source allowing acceptable analysis errors. Considering that a narrow-band filter due to a high-Q resonator on the primary side passes the resonant-frequency component and suppresses the other components, the part of the circuit preceding the rectifier is regarded as an ideal sinusoidal voltage source when $|Z_\ell|$ reaches 0. Similarly the latter assumption gives good approximation when $|Z_\ell| \gg R_r$, that is,

a circuit connected forward to the rectifier can be regarded as a sinusoidal current source. Here a smoothing element in bridge rectifier is considered. Note that the choke inductor L_c fixes the load current I_L, and hence $i_{r,in}$ must be a square waveform, which is incompatible with the assumption of a sinusoidal current. Eventually, the capacitor C_c is compatible when $|Z_\ell| \gg R_r$ and the inductor L_c should be used when $|Z_\ell| \ll R_r$ for good approximation. We exploit the choke L_c considering the circuit structure connect forward to the rectifier, which will be designed later.

Figure 2 illustrates the assumed waveforms in case the choke L_c is used. $\theta = \omega_{ZR} t$ represents the angular time. When $0 \le \theta < \pi$, the input current $i_{r,in} > 0$ then the diodes D_1, D_4 are turned on, and D_2, D_3 are on the off-state. The on/off status becomes the opposite when $\pi \le \theta < 2\pi$. We assumed that the diodes on the on-state can be replaced with the DC voltage source whose voltage is V_F, which equals to the forward voltage drop of the diodes, and the resistance of the off-state diodes is infinity. Under the assumptions, the voltage of the left-side node of the inductor $v_{r,out}$ becomes full-wave rectified waveform as illustrated in the figure. Since the average voltage of an inductor is zero,

$$V_L = \frac{1}{\pi}\int_0^{\pi} \left(V_{r,in}\sin\theta - 2V_F\right) d\theta = \frac{2}{\pi}V_{r,in} - 2V_F \tag{16}$$

holds. Substituting Eq. (15) into the above equation yields

$$V_{L,est} = \frac{2I_1 R_{r,est}}{\pi}\sqrt{\frac{R_{in,ZR} - r_1}{R_2}\frac{1}{(CR_{r,est})^2 + D^2}} - 2V_F. \tag{17}$$

The estimated load voltage is V_L obtained by substituting the estimated load value computed with Eq. (11), the measured value of I_1 and $R_{in,ZR}$ into the above formula. All of the parameters in Eq. (17) are known on the primary side.

3. Design of reactance two-port matching circuit

3.1 limitation of power transfer efficiency

From the view point of the voltage estimation, the structure and parameters of the reactance two-port circuit are arbitrary while inappropriate design degrades power transfer efficiency. Here we consider the design of the reactance two-port circuit to improve power transfer efficiency as much as possible. We define the link efficiency η_{link} of the WPT circuit as the ratio of the power P_r consumed at the equivalent input resistance R_r in Fig. 1 (b) to the input power:

$$\eta_{link} \stackrel{\text{def}}{=} \frac{P_r}{\mathrm{Re}[v_1\overline{i_1}]} = \frac{P_r}{P_r + P_1 + P_2} = \left(1 + \frac{P_{ESR}}{P_r}\right)^{-1} \tag{18}$$

where P_{ESR} represents the sum of the power P_n consumed at the n-th side ESR. The same analysis as Ref. [22] gives the condition of secondary-side input impedance $Z_2 = R_2 + jX_2$ to maximize η_{link},

$$X_2 = 0, \tag{19}$$

and

$$R_2 = R_{2,opt} = r_2\left(1 + \sqrt{1 + k^2 Q_1 Q_2}\right), \tag{20}$$

which is uniquely determined with a coupling coefficient k and the quality factor of the n-th side inductor Q_n. In addition, the angular frequency ω must be satisfied

$$\omega = \omega_{opt}, \tag{21}$$

which is the angular frequency at which $Q_1 Q_2$ becomes maximum, since Q_n has peak value at particular frequency due to skin effect. When Eqs. (19)-(21) are satisfied, the limit of the link efficiency

$$\eta_{limit} = \frac{\sqrt{1 + k^2 Q_1 Q_2} - 1}{\sqrt{1 + k^2 Q_1 Q_2} + 1} \tag{22}$$

is achieved [22], [23]. η_{limit} gives the physical limit of power transfer efficiency determined with a position and specifications of transfer coils.

3.2 Design for maximizing normalized efficiency

Since η_{limit} monotonically increases as the kQ product increases, designing coils the kQ product of which becomes as large as possible leads to higher efficiency. However, designing coil is somewhat different from the task of circuit designers. From the standpoint of circuit design, we consider the circuit to maximize efficiency with the specified coil parameters, that is, η_{limit} is given in advance and is cannot be changed. In other words, our design aims that the normalized efficiency

$$\gamma \stackrel{\text{def}}{=} \frac{\eta_{link}}{\eta_{limit}} \tag{23}$$

to be 1. γ represents the "utilization ratio of the limitation efficiency", and is useful to compare circuit performances excepting coil abilities.

For γ to be 1, Eqs. (19)-(21) must be satisfied. Since only one parameters set of R_r and k can satisfy the equations, it is considered that the design of the reactance two-port circuit with target load $R_{r,t}$ and the target coupling coefficient k_t. According to the theory of image impedance [19], the conditions of parameters for satisfying Eqs. (19) and (20) are given by

$$\sqrt{\frac{B_o D_o}{A_o C_o}} = R_{r,t} \tag{24}$$

$$\sqrt{\frac{A_o B_o}{C_o D_o}} = R_{2opt,t} - r_2 = r_2\sqrt{1 + k_t^2 Q_1 Q_2} \tag{25}$$

where A_o represents the abbreviation for A at $\omega = \omega_{opt}$, and the same is true of B, C and D.

Equation (24) is a function of the equivalent input resistance of the rectifier $R_{r,t}$, while using a DC load target $R_{L,t}$

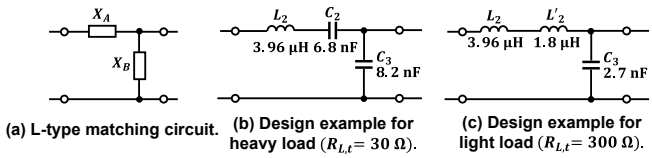

Fig. 3 Design examples of reactance two-port circuit.

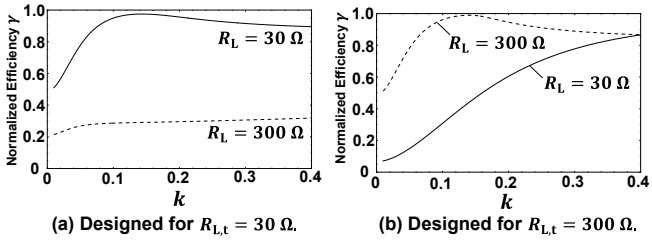

Fig. 4 Theoretical curves of normalized efficiency γ.

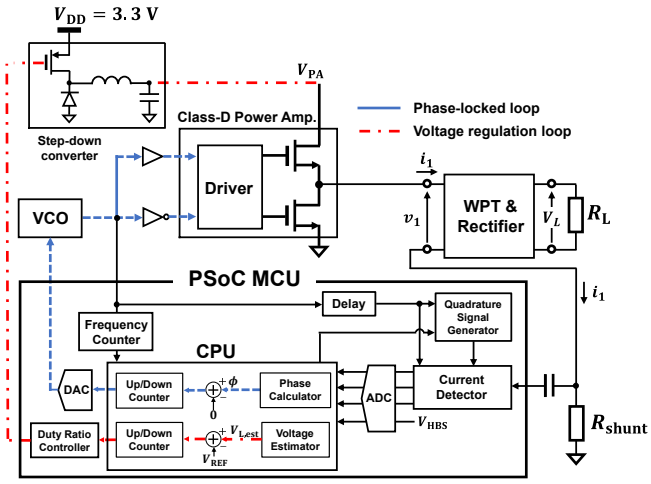

Fig. 5 Load voltage estimation and regulation system.

instead of $R_{r,t}$ provides a more useful design formula. The relationship between these parameters is derived here. Since the rectifier input current $i_{r,in}$ is a square wave the amplitude of which is $I_L = V_L/R_L$ as shown in Fig. 2, the amplitude of the fundamental frequency component of $i_{r,in}$ is equal to $(V_L/R_L) \cdot (4/\pi)$. The second factor $4/\pi$ is a coefficient of the first-order term of a Fourier series expansion. The rectifier's equivalent input resistance for fundamental frequency component is expressed as

$$R_r = \frac{\pi}{4}\frac{V_{r,in}}{V_L}R_L. \tag{26}$$

Eliminating $V_{r,in}$ using Eq. (16), and assuming that the load voltage V_L is regulated for V_{REF}, yields

$$R_{r,t} = \frac{\pi^2}{8}\left(1 + \frac{2V_F}{V_{REF}}\right)R_{L,t}. \tag{27}$$

Substituting Eqs. (20) and (27) into Eqs. (24) and (25) gives the conditions of the $ABCD$ parameters so that γ to be 1 with the specified target parameters $R_{L,t}$ and k_t.

3.3 Design example

There are many possible configurations of the reactance two-port circuit that satisfy Eqs. (24) and (25). As an example, an L-type matching circuit as shown in Fig. 3 (a) is exploited here. X_A and X_B are two-terminal networks realized by inductors and capacitors including the receiving inductor L_2. Substituting the $ABCD$ parameters of an L-type circuit into Eqs. (24) and (25) yields

$$X_A = \mp\sqrt{R'_{2opt,t}\left(R_{r,t} - R'_{2opt,t}\right)} \tag{28}$$

$$X_B = \pm R_{r,t}\sqrt{\frac{R'_{2opt,t}}{R_{r,t} - R'_{2opt,t}}} \tag{29}$$

where $R'_{2opt,t} = R_{2opt,t} - r_2$. Figure 3 (b) and (c) show the design examples for $R_{L,t} = 30\,\Omega$ and $300\,\Omega$, respectively, with the specified receiver coil parameters shown in Table 1, $k_t = 0.17$, and $V_{REF} = 1.8\,V$. $k_t = 0.17$ is the coupling coefficient of the coils used in later experiments with an inter-coil distance d of around 7 mm. This distance represents the midpoint between 4 mm and 10 mm, which are nominal variations in the thickness of human skin [1]. $R_{L,t} = 30\,\Omega$ is set so that the load power is around 100 mW when $V_L = V_{REF} = 1.8\,V$. Figure 4 (a) and (b) show the theoretical curves of the normalized efficiency γ of the circuits using the examples shown in Fig. 3 (b) and (c), respectively. In the figures γ for the case of the load with a target value becomes larger than that for other cases and takes the maximum at $k \simeq k_t = 0.17$. The figures validate the design formulas of Eqs. (27) - (29) and highlights the importance of designing the matching circuit to correspond to the specific load value of applications.

The optimum parameters are derived from Eqs. (20) and (27)-(29) in accordance with target applications. For instance, if a load circuit operates under the heavy-load condition of $R_L = 30\,\Omega$ for longer time than under light-load conditions, the circuit of Fig. 3 (b) should be chosen. The circuit (b) will be adopted as an example in the experimental section.

4. Load voltage estimation and regulation system

4.1 overall configuration

Figure 5 shows a proposed voltage regulation system. The circuit block labeled "WPT & Rectifier" is the same as the two-port circuit shown in Fig. 1 (a) except for the source and the load. The system consists of two feedback loops: a phase-locked loop (PLL) and a voltage regulation loop. The current detector detects the magnitude and the phase of the input current i_1 for these feedback control. The detail of the each circuits and the loops will be described later.

As shown in the figure, most of the components for control such as the analog-to-digital converter (ADC), the

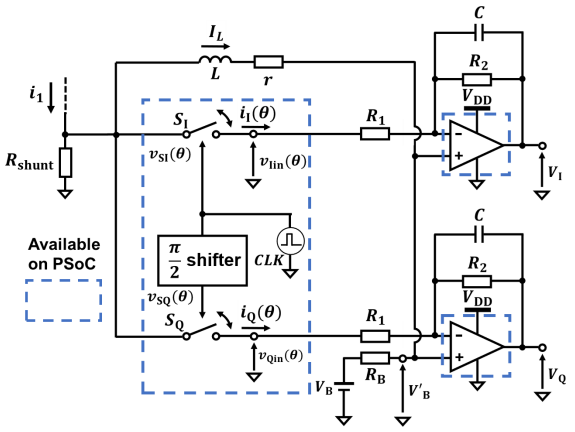

Fig. 6 Current detector.

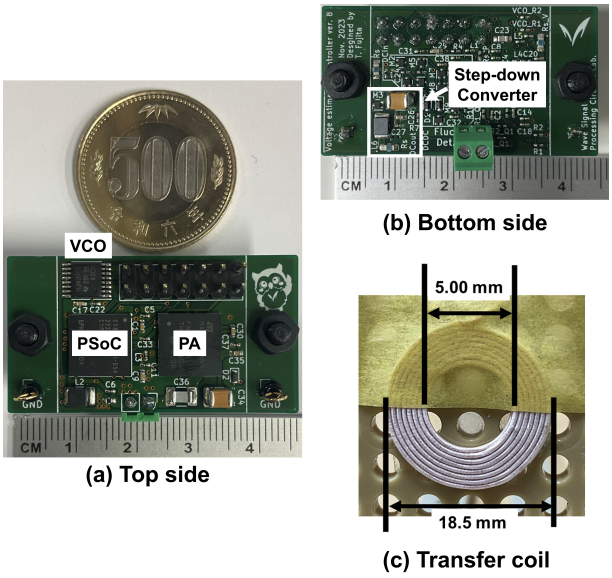

Fig. 7 Photos of primary-side circuit implemented on PCB (a), (b) and transfer coil (c).

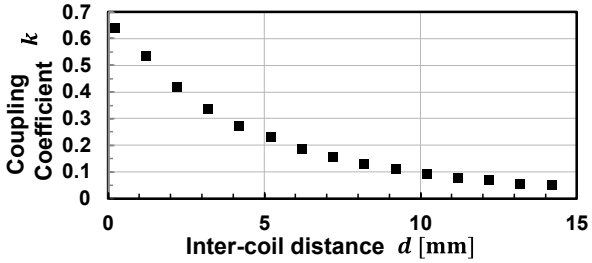

Fig. 8 Measured relationships between inter-coil distance d and coupling coefficient k.

frequency counter, and the versatile central processing unit (CPU) are implemented with the off-the-shelf programmable system-on-chip (PSoC) microcontroller unit (MCU). PSoC contains various analog and digital circuit blocks, the connections and configurations of which can be programmed by software. We adopt a PSoC not only because it facilitates easy prototyping but also because it is suitable for small-lot applications that are unsuitable for implementation with an application-specific integrated circuit (ASIC).

4.2 current detector

A current detector proposed in Ref. [24] is utilized here. As shown in Fig. 6, it consists of two switches controlled by quadrature signals, and two active low-pass filters (LPFs). The current i_1 is converted to the voltage with the shunt resistor R_{shunt}, and then applied to the detector. The quadrature signal is generated from the drive signal of the class-D power amplifier (PA). Both the current amplitude I_1 and the phase difference ϕ between the drive signal and i_1 are obtained thanks to the principle of coherent detection. These parameters are known from the DC output voltages of the operational amplifiers V_{I}, V_{Q} and the bias voltage V'_B as

$$\phi = -\tan^{-1}\frac{V_{\text{Q}} - V'_{\text{B}}}{V_{\text{I}} - V'_{\text{B}}}, \tag{30}$$

$$I_1 = \frac{\pi}{A_0}\frac{V_{\text{I}} - V_{\text{Q}}}{R_{\text{shunt}}}\frac{\sqrt{1+\tan^2\phi}}{1+\tan\phi}\left(1+\frac{R_{\text{on}}}{R_1}\right) \tag{31}$$

where $A_0 = -R_2/R_1$ represents the DC gain of the LPFs and R_{on} does the on-resistance of the switches. A detailed analysis is available in Ref. [24].

4.3 phase-locked loop

A phase-locked loop (PLL) is illustrated with the dashed line in Fig. 5. The PLL works so that the phase difference ϕ to be 0 by adjusting the control voltage of the voltage controlled oscillator (VCO). The value of ϕ is computed by the CPU using Eq. (30) with the measured values of the voltages obtained by the ADC. The output value of the up-down counter, which works as an accumulator, is incremented or decremented depending on the sign of ϕ. The digital-to-analog converter (DAC) converts the counter value to the analog voltage, which is applied to the VCO. This control loop result in ϕ to be 0, that is, the VCO output frequency is controlled so that the input impedance seen from the PA becomes purely resistive.

4.4 voltage regulation loop

The dot-dashed line in the figure illustrates the voltage regulation loop, which controls the output power of the PA so that the estimated load voltage $V_{\text{L,est}}$ to be the reference voltage V_{REF}. The power control is realized by adjusting the duty ratio of the control signal applied to the step-down converter. The duty ratio is determined with the value of the up-down counter, which accumulates the difference of V_{REF} and $V_{\text{L,est}}$ computed by the CPU. The source voltage of the PA V_{PA} is appropriately adjusted as a result of the feedback control.

Table 1 List of implemented elements.

element	nominal value / part number	measured value	usage / note
IC1	PSoC MCU CY8C6247BZI-D54	-	control
IC2	CD74HC4046	-	VCO
IC3	MasterGan4	-	PA
L_1	4.1 μH	4.07 μH	transmission coil
r_1	-	0.900 Ω	ESR of L_1
Q_1	-	33.2	quality factor of L_1 †
C_1	3.9 nF	3.89 nF	resonance capacitor
R_{shunt}	100 mΩ	-	current detection
L_2	4.1 μH	3.96 μH	receiving coil
r_2	-	0.867 Ω	ESR of L_2
Q_w	-	37.3	quality factor of L_2
C_2	6.8 nF	6.72 nF	matching circuit
C_3	8.2 nF	8.10 nF	matching circuit
$D_1 - D_4$	BAT60A $V_F = 0.12$ V‡	-	rectification
L_c	100 μH	-	smoothing
r_c	2.70 Ω	-	ESR of L_c

†calculated including R_{shunt}.
‡Typical value at 10- mA of the diode current.

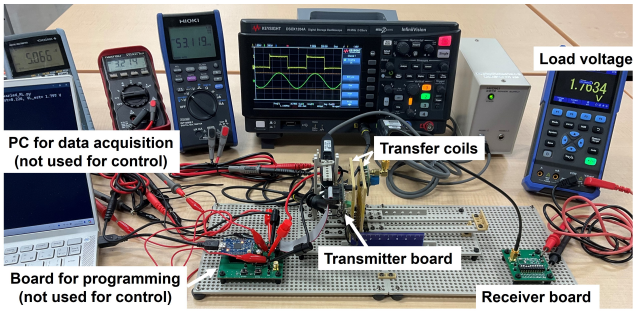

Fig. 9 Experimental setup.

5. Experimental results

The prototype implementation to validate the proposed system is designed using some off-the-shelf integrated circuits and discrete components. Figure 7 (a) and (b) shows the primary-side circuit (transmitter) of the proposed system implemented on an one-coin size 4-layer printed circuit board (PCB). The secondary-side circuit is implemented on the another PCB with four diodes for rectification and two capacitors for the matching circuit. The same specification coils shown in Fig. 7 (c) are used on both the primary and the secondary sides. Table 1 summarizes part numbers or values of the implemented elements. The value of each elements are measured at $f = f_{\text{opt}} = \omega_{\text{opt}}/(2\pi) = 1.3$ MHz. Figure 8 shows the measured relationships between the coupling coefficient k and the inter-coil distance d. The overall experimental setup is shown in Fig. 9.

The system performance measured at several values of R_{L} and k. Figure 10 shows the measured waveform of the PA's output voltage v_1, the current i_1, and the product of them (instantaneous input power) for the later efficiency evaluation at $R_{\text{L}} = 60\,\Omega$ and $k \simeq 0.17$ ($d = 7.2$ mm). The figure validates the operation of the PLL since v_1 and i_1 are in-phase. Figure 11 (a) shows the ratio of the measured load

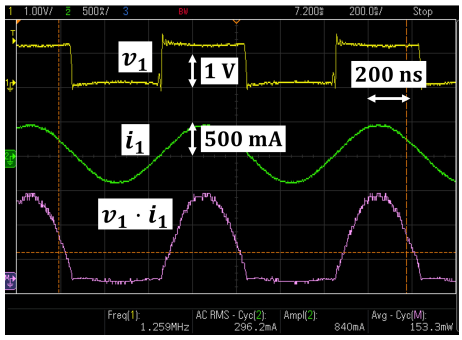

Fig. 10 Measured waveforms.

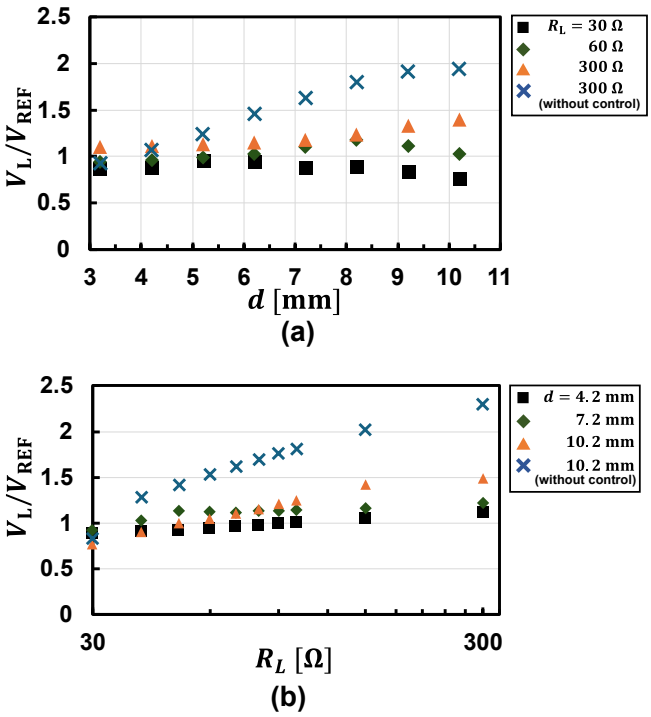

Fig. 11 Measured load voltage normalized with V_{REF}.

voltage V_{L} to the reference voltage $V_{\text{REF}} = 1.8$ V for varied values of d in case of three load conditions: $R_{\text{L}} = 30\,\Omega$, 60 Ω, and 300 Ω. The plots marked with "×" are the results without the control for comparison and the others are with control. Without control, the load voltage V_{L} strongly depends on d, whereas the voltage fluctuation is effectively suppressed when control is enabled. The voltage error under the control is relatively large when both of the load and the distance are large, that is, a light load and a weak coupling are prone to degrade the estimation accuracy. This is also confirmed in Fig. 11 (b), which is the measurement results with the load R_{L} varied with three different values of d.

Our design aim is to maximize the normalized efficiency $\gamma = \eta_{\text{link}}/\eta_{\text{limit}}$ at the target load $R_{\text{L,t}}$ and the coupling coefficient k_{t}, as described in Sect. 3. Figure 12 shows the measurement results of γ and its theoretical curves. η_{link} is obtained as the ratio of the power consumed at the equivalent resistance P_{r} to the power delivered from the PA P_{PA}. Since

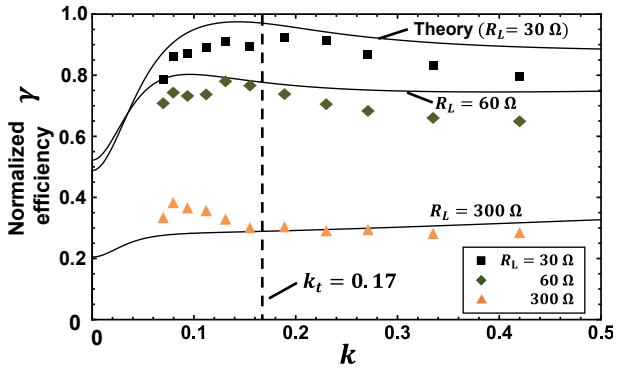

Fig. 12 Experimental and theoretical values of normalized efficiency γ.

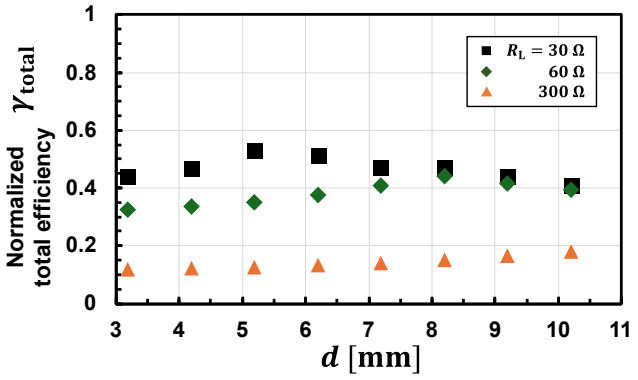

Fig. 13 Measurement results of normalized total efficiency γ_{total}.

P_{r} cannot be measured directly, it is estimated as

$$P_{\text{r}} = P_{\text{L}} + P_{\text{rect}} \tag{32}$$

where P_{L} is the measured value of the power consumed at R_{L}. P_{rect} is the dissipated power of the rectifier and the choke inductor, which is approximated as

$$P_{\text{rect}} \simeq 2V_{\text{F}}I_{\text{L}} + I_{\text{L}}^2 r_{\text{c}} \tag{33}$$

since the effective value of the current flowing through one of the rectification diodes is approximately $I_L/2$, and the ESR of the choke L_{c} is connected in series to the load. P_{PA} is derived by computing the mean value of the measured waveform of $v_1 \cdot i_1$. In Fig. 12 the theoretical curves are well matched to the measured values. For the case of the target load that R_L becomes equal to $R_{\text{L,t}} = 30\,\Omega$, γ reach to approximately 1 at $k = k_{\text{t}}$ as designed. The peak value is slightly lower than 1 because the curve is computed with the measured values of the implemented elements. The measured values become maximum at $k = 0.19$, which is closed to the specified target value $k_t = 0.17$, and $R_{\text{L}} = R_{\text{L,t}}$. This suggests that the validity of the design formulas derived in Sect. 3.

Table 2 Comparision with previous works.

Jounal	TBCAS [14]	JSSC [16]	JSSC [12]	JSSC [15]	ISSCC [17]	This Work
Year	2015	2015	2018	2021	2021	-
Detection coil	YES	YES	YES	YES	NO	NO
Frequency [MHz]	13.56	13.56	13.56	6.78	6.78	1.09~1.25
Max. load power [mW]	234	102	38.4	400	32	99.8
Max. total efficiency $\eta_{\text{total,max}}$ (%)	62.4 @ d = 0.3 cm, P_{L}= 80 mW	50 @ d = 0.3 cm, P_{L}= 60 mW	69 @ d = 0.6 cm, P_{L}= 38.4 mW	71.5 @ d = 0.3 cm, P_{L}= 400 mW	61.9 @ d = 0.65 cm, P_{L}= 22.5 mW	39.9 @ d = 0.52 cm, P_{L}= 99.8 mW
Limit efficiency $\eta_{\text{limit}}^{\dagger}$ (%)	84.4	81.4	89.1	97.3	90.9	74.9
Normalized efficiency $\gamma = \frac{\eta_{\text{link}}}{\eta_{\text{limit}}}$	-	-	-	-	-	0.891
Normalized total effi. $\gamma_{total} = \frac{\eta_{\text{total,max}}}{\eta_{\text{limit}}}$	0.739	0.614	0.774	0.735	0.681	0.533

†: Limit efficiency at the inter-coil distance d at which the $\eta_{\text{total,max}}$ becomes maximum.
The values are calculated with the authours by substituing the specified k and Q into Eq. (22).
In case the value of k is not specified, the authours estimated it by the Neumann's formula with the specified coil size.

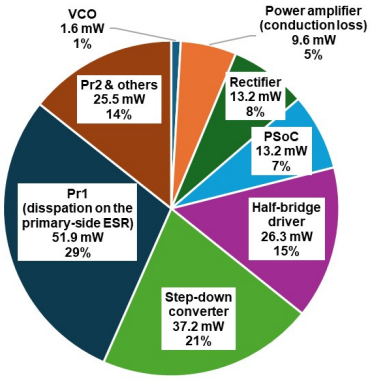

Fig. 14 Breakdown of power dissipation.

6. Discussion

6.1 power dissipation and its breakdown

It is desirable to compare the measured value of γ with conventional voltage regulation systems to specify the advantage of the proposed method. However γ cannot be compared with other systems because the previous researches did not measure the link efficiency η_{link}, which is necessary to calculate γ. Therefore we use the normalized total efficiency

$$\gamma_{\text{total}} \stackrel{\text{def}}{=} \frac{\eta_{\text{total}}}{\eta_{\text{limit}}} \tag{34}$$

for comparison where η_{total} is the ratio of the load power P_{L} to the power supplied from the DC voltage source on the primary side.

Figure 13 shows the measured value of γ_{total}. As shown in the figure, the maximum value of γ_{total} is approximately 0.53, which is relatively lower than the state-of-the-art voltage regulation system exploiting a regulated rectifier technique listed in Table 2.

To examine the cause of the efficiency degradation, we measured or estimated the power losses in each circuit block. Figure 14 summarizes the breakdown of the power dissipation when $R_{\text{L}} = 60\,\Omega$ and $d = 7.2\,\text{mm}$. This shows that

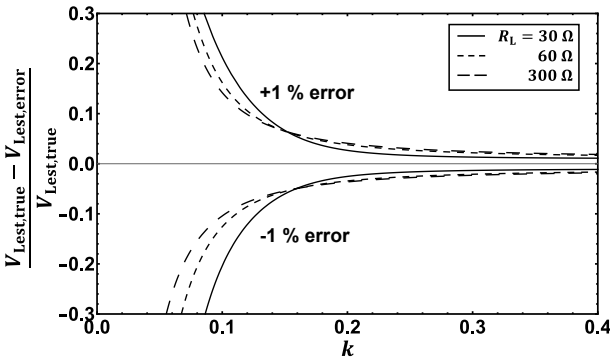

Fig. 15 Error of estimated voltage caused by frequency measurement error.

the power dissipated on the step-down converter and the external half-bridge driver IC is relatively large. The authors expect that the power dissipation of these components can be reduced by replacing them with other power-efficient circuit configurations. For example, exploiting intermittent operation of the PA is available for power control without the need for a step-down converter. The loss of the PA and its driver is also reducible by optimizing a transistor size for lowering on-resistance. A concrete design of the control circuitry is a future work.

6.2 voltage error

Figure 11 suggests that the load voltage is prone to have large error for weak coupling conditions. It is beneficial for applications design to estimate how large of the error before implementation. The load voltage error could be caused by various factors so it is difficult to consider all of them. Here we assume that the error is mainly caused by the measurement error of the frequency, as it is involved in almost all parameters used in the estimation such as $ABCD$ parameters. Figure 15 shows the calculation results of the error ratio $(V_{\mathrm{Lest,true}} - V_{\mathrm{Lest,error}})/V_{\mathrm{Lest,true}}$ for three values of R_{L}. $V_{\mathrm{Lest,true}}$ is calculated by substituting the theoretical value of ω_{ZR} derived by Eq. (6) into Eq. (17) and $V_{\mathrm{Lest,error}}$ is by the same procedure with ±1% error of ω_{ZR}. The figure shows that the magnitude of the error rate becomes larger as k decreases for all values of the load. Since this characteristics is roughly matched to the measurement results in Fig. 11, it is considered that the designers who would like to adopt the proposed method can roughly estimate the magnitude of the voltage error and its influences for their applications with the similar calculation.

The experimental results confirm that the proposed system can regulate the load voltage without an external coil for intercommunication, and that the normalized efficiency is maximized at desired parameter values. On the other hand, it is also suggested that there is still room for reducing the power dissipation of the control circuitry to enhance system efficiency.

7. Conclusion

This paper proposes a load voltage regulation system for WPT circuits only using primary-side control. The load voltage estimation without feedback communication is achieved thanks to the adaptive frequency control utilizing a PLL. Design formulas for the secondary-side reactance two-port circuit to maximize power transfer efficiency at desired load and coupling conditions are provided. Vesatile and explicit design formulas can be adopted for various applications and are beneficial for design without complicated parameters adjustments. The prototype implementation confirms a voltage regulating operation and validates the design formulas.

To design more energy-efficient control circuitry is a future work. We expected that introducing intermittent operation in the PA and implementing a power-saving mode of the entire control circuitry during stable conditions are promising to lower power losses. Also to enhance the accuracy of estimated load voltage is a future work.

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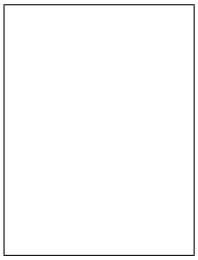

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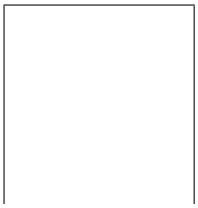

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