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# Highly Reliable Non-volatile Logic Circuit Technology and Its Application

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**SUMMARY** A ferroelectric-based (FE-based) non-volatile logic is proposed for low-power LSI. Standby currents in a logic circuit can be cut off by using FE-based non-volatile flip-flops (NVFFs), and the standby power can be reduced to zero. The FE capacitor is accessed only when the power turns on/off, performance of the NVFF is almost as same as that of the conventional flip-flop (FF) in a logic operation. The use of complementarily stored data in coupled FE capacitors makes it possible to realize wide read voltage margin, which guarantees 10 years retention at 85 degree Celsius under less than 1.5V operation. The low supply voltage and electro-static discharge (ESD) detection technique prevents data destruction caused by illegal access for the FE capacitor during standby state. Applying the proposed circuitry in CPU, the write and read operation for all FE capacitors in 1.6k-bit NVFFs are performed within 7$\mu$s and 3$\mu$s with access energy of 23.1nJ and 8.1nJ, respectively, using 130nm CMOS with $Pb(Zr,Ti)O_3$(PZT) thin films.

***key words:*** *non-volatile logic, non-volatile flip-flop, ferroelectric capacitor, high reliability, data protection*

## 1. Introduction

Low power logic circuits have been attracting more and more attentions with the rapid spread of LSI applications such as mobile electronics. And the reduction of standby power is one of critical issues for low power LSI since the leakage current greatly increases with downscaling of technology node [1]–[3].

Recently, the technology of non-volatile logic (NVL) using non-volatile flip-flops (NVFF) has been proposed as one of the promising candidates to solve the above problem [4], [5]. In the NVL, all registers consist of NVFFs which have capability to retain its state without power supply. Therefore, it is possible to cut off the power supply during standby state, and standby power is reduced to zero. The NVL technology is very suitable not only for low-power LSI but also for energy harvesting applications such as infrastructure and building automation because it is capable of continuously operating a logic circuit and retaining state during frequent power interruption, i.e., unstable power supply. An arbitrary logic circuit is easily nonvolatized by replacing all conventional flip-flops (FFs) to NVFFs.

An important point of NVL circuit design is to implement an NVFF without performance degradation in comparison with a conventional FF. If an NV device implemented in the NVFF acts as an additional load device in the logic operation, it causes large loss of the dynamic power.

To overcome the above issue, this paper presents a ferroelectric-based (FE-based) NVL circuit, in which the NVFF is designed on the basis of conventional FF circuits with FE capacitors and access drivers. Since FE capacitors are isolated by disabled access driver except for turning on/off the power supply, performance of the NVFF is almost as same as that of the conventional FF during a logic operation. The access sequence for FE capacitors in all NVFFs is controlled by an NVFF controller jointly working with a reset IC or a power-on-reset (POR) circuit, which is used to detect turning on/off of the power supply [6], [7]. Since FE capacitors are accessed only when the NVFF controller detects a positive/negative edge of the reset signal, access times of FE capacitors are same to the cycles of power ON/OFF cycle. Therefore, regarding the fatigue endurance of $10^{12}$ cycles of FE capacitors [8], the NVL is able to bear a 10 year long performance assuming power ON/OFF happening 3000 times in a second. Moreover, the use of complementarily stored data in coupled FE capacitors makes it possible to realize wide read voltage margin [9], which guarantees 10 years retention at 85 degree Celsius without power supply after low voltage operation of $V_{DD}$ < 1.5V. Characteristics of all FE capacitors can be evaluated by using comparators in NVFFs together with a scan path, and it is possible to screen out the anomalous FE capacitors, which have a signal margin less than quality assurance level.

In addition, two kinds of data protection technique are introduced to the NVFF controller for the reliable operation. One is a voltage-level checker (VLC), which is used to protect stored data in FE capacitors from an illegal operation caused by an incorrect signal coming from the POR during rising of $V_{DD}$. The VLC is able to forbid any operation if $V_{DD}$ is lower than the specified detect voltage $V_{detV}$. Since the required accuracy of $V_{detV}$ is low, the VLC can be constructed by a simple circuit. The other is an electro-static-discharge(ESD) detection technique by checking the voltage level on multi PADs, which can prevent an illegal access for FE capacitors caused by ESD.

The proposed NVL technology has been already applied to several applications such as an NV counter, a reconfigurable logic and a non-volatile CPU (NVCPU) [10]–[12]. The NVCPU demonstrates that the write and read operations for all FE capacitors in 1.6K NVFFs are performed by 7$\mu$s and 3$\mu$s with access energy of 23.1$n$J and 8.1$n$J, re-

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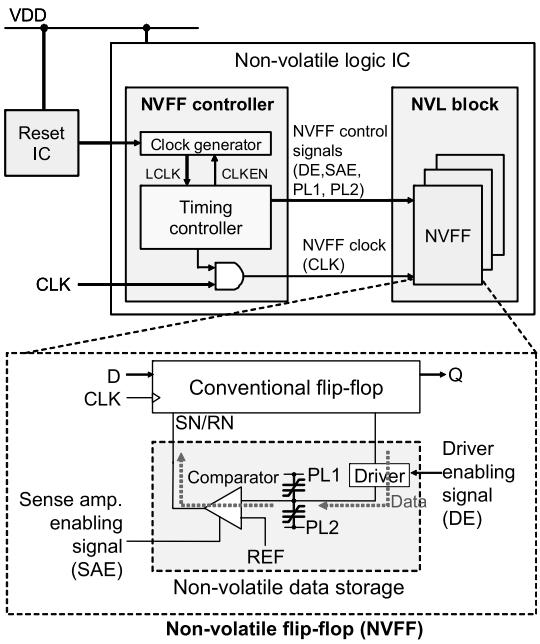



**Fig. 1** Overall structure of a non-volatile logic circuit.

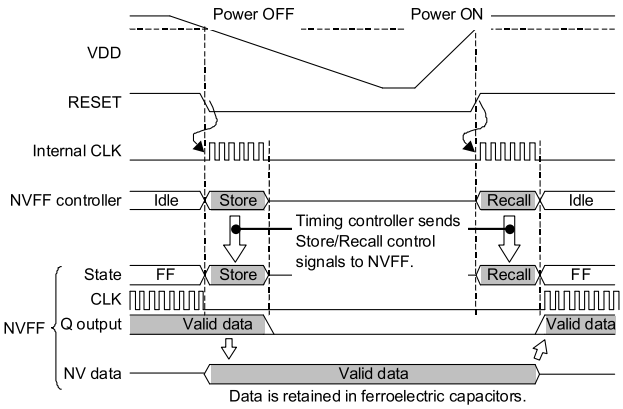



**Fig. 2** Basic operation of a non-volatile logic circuit.

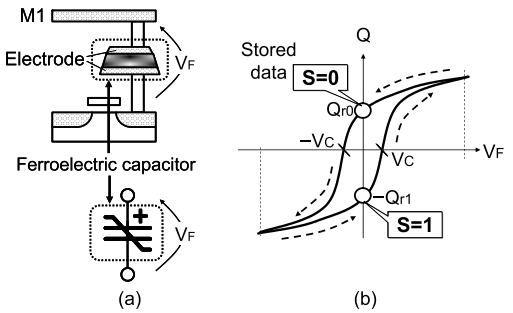



**Fig. 3** Ferroelectric capacitor. (a) Cross-sectional view and Symbol. (b) Hysteresis loop characteristic.

spectively, using 130nm CMOS with $Pb(Zr,Ti)O_3$(PZT) thin films.

## 2. Non-volatile Logic Circuit

### 2.1 General Structure

Figure 1 shows the general structure of an NVL circuit, which consists of three components, non-volatile flip-flops (NVFFs), a clock generator and a timing controller. The NVFF is designed on the basis of a conventional FF circuit with FE capacitors. The write driver and comparator are controlled by a driver enabling signal DE and a sense-amplifier enabling signal SAE, respectively. These signals are controlled by the NVFF controller module, which is synchronized to a clock signal supplied by the clock generator.

Figure 2 shows a basic operation of the proposed NVL circuit. The NVFF controller is basically controlled by using reset signal, which comes from a reset IC or a POR circuit [6], [7]. When $V_{DD}$ reaches to the detect voltage $V_{detR}$ of the reset IC with turning on the power supply, a positive edge of the reset signal is applied to the NVFF controller. Simultaneously, the clock generator starts to generate clock signals for the timing controller, and the recall operation is performed. After reading out stored data from FE capacitors, the NVFF controller becomes idle mode, and the NV logic block performs a normal logic operation. In the same way, a store operation is enabled the negative edge of the reset signal as the power supply is turning off. Stored data in an FF circuit is written into the FE capacitors through the write driver in the NVFF, and then the NVL circuit becomes idle mode. At power on state, the NVFF works as a conventional FF. The write driver is constantly at high-impedance state with two plate lines PL1 and PL2 grounded. Since the applied voltage across the FE capacitor is kept at 0V, no power loss is induced by FE capacitors. Therefore, in the logic operation, performance of the NVFF is equal to that of the conventional FF.

### 2.2 Review of Ferroelectric Capacitors

The FE capacitor is a kind of a non-volatile storage devices, and it has been used as a memory cell of a ferroelectric random-access memory (FeRAM) [8]. The FE capacitor is physically distinguished from a regular capacitor by substituting the dielectric with an FE material as shown in Fig. 3 (a). When the voltage $V_F$ applied across the FE capacitor becomes higher than the coercive voltage $V_C$, the polarization charge $Q$ in the FE capacitor shows a hysteresis loop characteristic with a remnant-polarization charge $Q_r$ as shown in Fig. 3 (b). Since $Q_r$ is retained at $V_F = 0$, the FE capacitor is capable of a non-volatile memory device, where $Q_r$ is $Q_{r0}$ for a logic value "0" or $-Q_{r1}$ for "1".

Basically, stored data $S$ in the FE capacitor is read out by the capacitive coupling effect between the FE capacitor and a load capacitor. When $V_{DD}$ is applied to series-connected capacitors, an output voltage $V_{OUT}$ on an intermediate node is determined by ratio of $C_F$ to $C_L$ as shown in Fig. 4 (a), where $C_F$ and $C_L$ indicate equivalent capacitance of the FE capacitor and the load capacitor, respec-

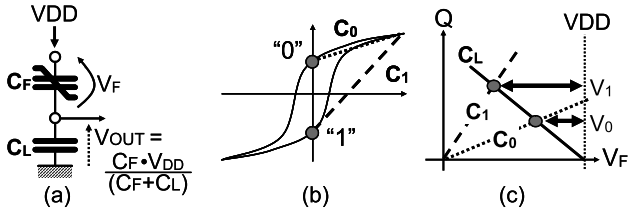



**Fig. 4** Read operation of the ferroelectric capacitor. (a) Equivalent read circuit. (b) Capacitance of the ferroelectric capacitor. (c) Output voltage caused by the capacitive coupling effect.

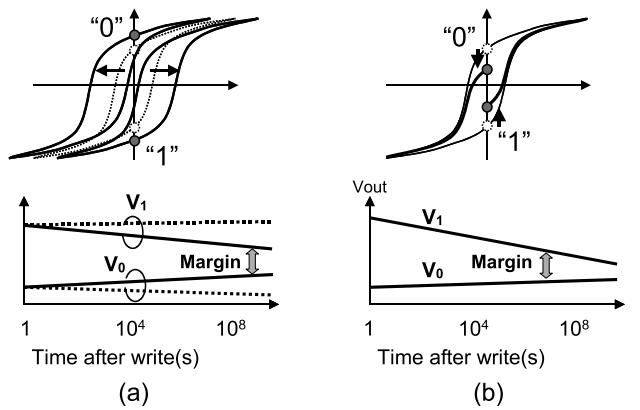



**Fig. 5** Imperfections of the ferroelectric capacitor. (a) Imprint. (b) Retention.

tively. Since $C_L$ becomes $C_0$ or $C_1$ depending on stored data $S$ as shown in Fig. 4 (b), $V_{OUT}$ becomes high $V_1$ for $S = 1$ or low $V_0$ for $S = 0$ as shown in Fig. 4 (c). Theoretically, a read voltage margin $\Delta V_{OUT} = V_1 - V_0$ is increasing as a function of $C_1/C_0$ ratio. In the case of $C_L = \sqrt{C_0 C_1}$, $\Delta V_{OUT}$ becomes maximum, which is expressed as

$$\Delta V_{OUT} = (\sqrt{C_1/C_0} - 1)/(\sqrt{C_1/C_0} + 1) \cdot V_{DD}. \quad (1)$$

In the use of the FE capacitors, it is important to consider the output voltage shift caused by various FE capacitor imperfections such as imprint and retention [8]. Imprint refers to an physical phenomenon that the polarization can be coerced to its initial direction easier than its opposite direction if the polarization state is statically kept for a long period of time as shown in Fig. 5 (a). Retention refers to a partial loss of remnant charge during power off as shown in Fig. 5 (b). These imperfections decrease $C_1/C_0$, which results in degradation of $\Delta V_{OUT}$.

### 2.3 Non-volatile Flip-Flop

In the implementation of the NVFF, it is important to realize large $\Delta V_{OUT}$ at $V_{DD} < 1.5$V because the store and recall operations are performed during falling and rising of $V_{DD}$, respectively. However, a conventional circuit based on Fig. 4 (a) is not suitable to be used in the NVFF because of its large overhead caused by the load capacitor, in which $C_L = \sqrt{C_0 C_1}$ usually becomes several hundred femtofarad.

In the proposed NVFF, coupled FE capacitors with

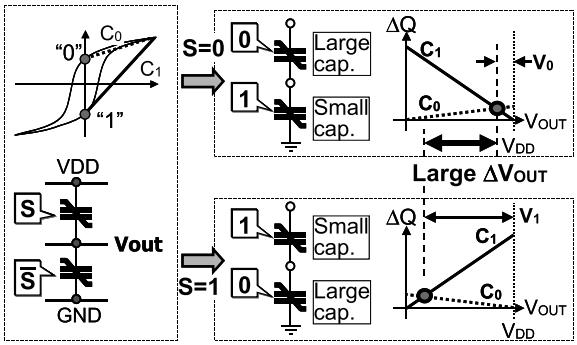



**Fig. 6** Capacitive coupling with complementary data storage.

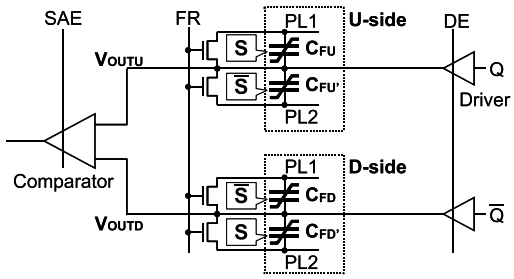



**Fig. 7** Schematic of a non-volatile data storage circuit included in the NVFF.

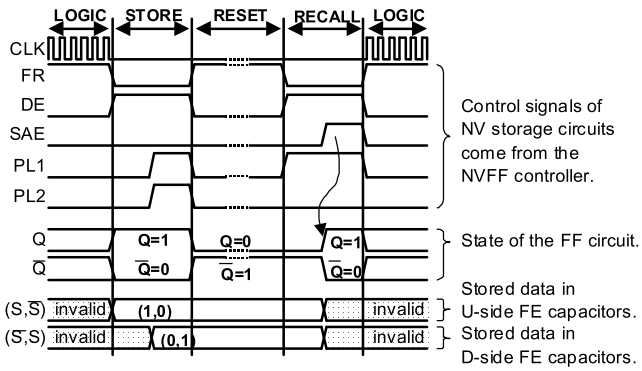



**Fig. 8** Timing diagram of a basic operation of the NVFF.

complementary data storage [9] are introduced to realize large $\Delta V_{OUT}$ with small area overhead. In this circuit, datum $S$ is stored into in series-connected FE capacitors as a pair of complementary code $(S, \bar{S})$ as shown in Fig. 6. Since capacitance of two FE capacitors changes complementarily depending on $(S, \bar{S})$, large $\Delta V_{OUT}$ can be obtained by capacitive coupling, in which $\Delta V_{OUT}$ is represented as

$$\Delta V_{OUT} = (C_1/C_0 - 1)/(C_1/C_0 + 1) \cdot V_{DD}. \quad (2)$$

For example, in the case of $C_1/C_0 = 2$, $\Delta V_{OUT}$ in (2) becomes 33% of $V_{DD}$, which is twice of 17% of $\Delta V_{OUT}$ in (1). This circuit is implemented only by FE capacitors without the large load capacitor, its circuit area becomes small in comparison with the conventional one.

Figures 7 and 8 show a schematic and a timing diagram of a basic operation of the proposed NVFF, respectively. In

**Table 1** Relationship between stored data in FE capacitors and the read voltage corresponding to state $Q$ of the FF circuit.

| | Stored Data | | | | Read Voltage | |
|---|---|---|---|---|---|---|
| | U side | | D side | | U side | D side |
| Q | $C_{FU}$ | $C_{FU'}$ | $C_{FD}$ | $C_{FD'}$ | $V_{OUTU}$ | $V_{OUTD}$ |
| 0 | 0 | 1 | 1 | 0 | $V_0$ | $V_1$ |
| 1 | 1 | 0 | 0 | 1 | $V_1$ | $V_0$ |

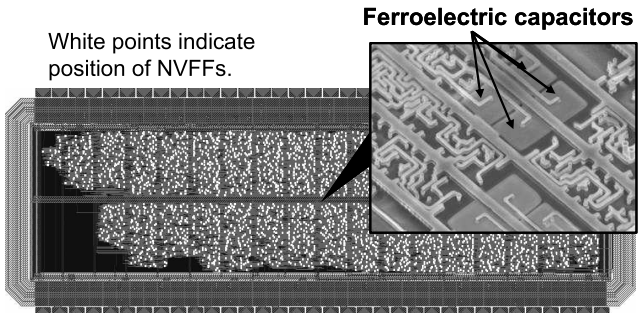



**Fig. 9** 4096 NVFFs-chained test circuit.

the logic operation, the NV data storage circuit is separated from the FF circuit by the disabled write driver and comparator. In the store operation, the clock signal for the FF is stopped by the NVFF controller, and write drivers are enabled by a driver enabling signal, DE. Then, the state $Q$ in the FF circuit is written into U-side and D-side of series-connected FE capacitors as pairs of complementary code $(S, \bar{S})$ and $(\bar{S}, S)$, respectively. Table 1 shows the relation between $Q$ and stored data in FE capacitors.

In the reset state, FE capacitors are separated from the FF circuit. During the transience of power on/off, the NVFF will also undergo voltage turbulence at $V_{DD}$, due to which the voltage applied on the FE capacitor might lead to a datum destruction. To prevent it from happening, all FE capacitors are shorted by parallel-connected MOS transistors with PL1 and PL2 grounded. In the recall operation, voltage pulse is applied to PL1 with PL2 grounded. Simultaneously, $V_{OUTU}$ and $V_{OUTD}$ are induced by capacitive coupling of D-side and U-side FE capacitors, respectively. Then, $V_{OUTU}$ and $V_{OUTD}$ are compared by the comparator, and the FF circuit is set or reset depending on the comparison result.

Characteristic of the proposed NVFF is evaluated by using a 4096 NVFFs-chained circuit. A test chip is fabricated by using 130nm CMOS with Pb(Zr,Ti)$O_3$(PZT) thin films. All NVFFs are randomly placed on a logic circuit as shown in Fig. 9, and two series-connected FE capacitors are arranged as 2 by 2 array in the NVFF. Figure 10 (a) and (b) show the relation between $V_{OUT}$ and $V_{DD}$, and $V_{OUT}$ distribution of the 4096 NVFFs-chained circuit. The read voltage margin $\Delta V_{OUT}$ becomes larger than 400mV at $V_{DD}$ =1.5V. But it would gradually degrade due to the imprint and relaxation, and it was extrapolated that the $\Delta V_{OUT}$ was still larger than 90mV after being baked at 85 degree Celsius for 10 years as shown in Fig. 11, which is large enough to perform reliable store and recall operations at $V_{DD}$ < 1.5V. In the retention time of a few milliseconds, the proposed NVFF

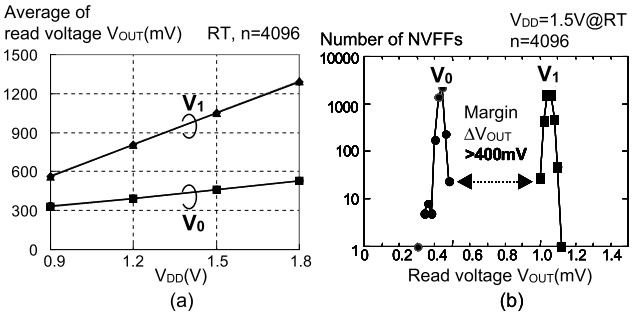



**Fig. 10** Read voltage $V_{OUT}$ of the NVFF. (a) Relationship between $V_{OUT}$ and $V_{DD}$. (b) $V_{OUT}$ distribution of a 4096 NVFFs-chained circuit.

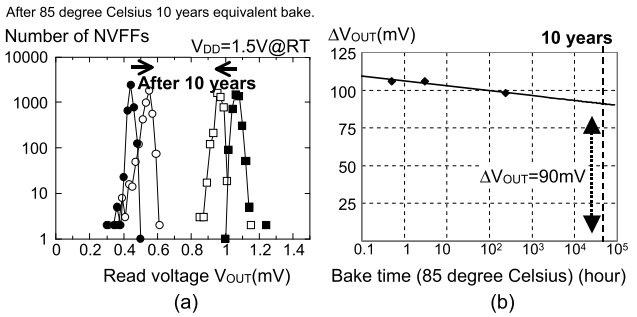



**Fig. 11** Read voltage $V_{OUT}$ after 10 years equivalent bake at 85 degree. (a) Imprint. (b) Retention.

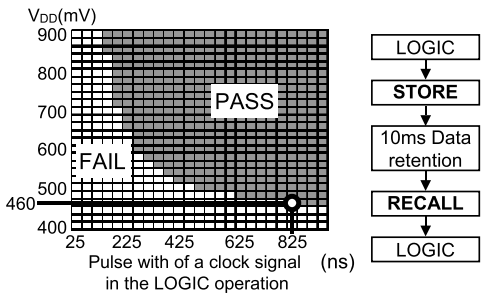



**Fig. 12** Shmoo plot.

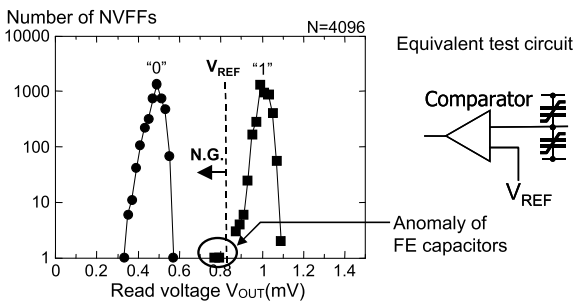



**Fig. 13** Screening test for anomaly of FE capacitors.

works at $V_{DD}$ < 0.5V as shown in Fig. 12.

Inferior NVFFs which have $\Delta V_{OUT}$ less than quality assurance with anomaly of FE capacitors can be easily rejected in the proposed NVFF. Applying analog voltage $V_{REF}$ to the comparator as shown in Fig. 13, the voltage level

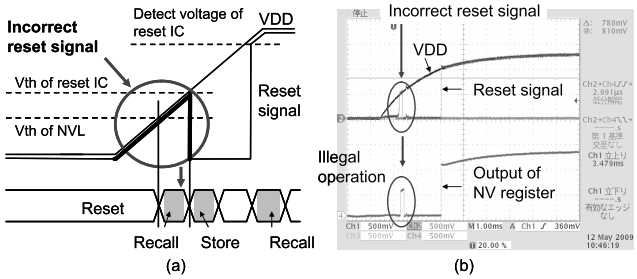
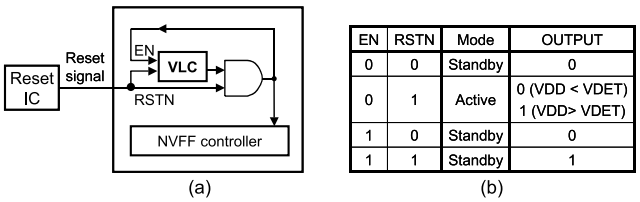



**Fig. 14** Behavior of the reset IC during rising of $V_{DD}$. (a) Incorrect reset signal. (b) Measurement result of an illegal operation.




| EN | RSTN | Mode | OUTPUT |
|---|---|---|---|
| 0 | 0 | Standby | 0 |
| 0 | 1 | Active | 0 (VDD < VDET)<br>1 (VDD> VDET) |
| 1 | 0 | Standby | 0 |
| 1 | 1 | Standby | 1 |

(b)

**Fig. 15** Voltage-level checker (VLC). (a) Block diagram of NVFF controller with the VLC. (b) Truth table of the VLC.

of $V_{OUT}$ can be compared to $V_{REF}$. Therefore, abnormal $V_{OUT}$ is found out by checking a comparison result with $V_{REF}$, which is set to quality assurance level of $V_{OUT}$. Since the comparison result is written into the FF circuit, inferior NVFFs are screened out by a scan path testing.

## 3. NVFF Controller with Highly Reliable Operation

The proposed NVFF has capability to work at $V_{DD} < 0.5$V. This characteristic sometimes becomes account for data destruction because the NVFF works illegally by an unexpected noise on input signals or $V_{DD}$. Therefore, the NVFF controller has to protect stored data in FE capacitors from above illegal operation.

### 3.1 Noise Protection

During rising of $V_{DD}$, an incorrect reset signal sometimes comes from the reset IC or POR when $V_{DD}$ is lower than the threshold voltage of the reset IC or POR as shown in Fig. 14 (a). Usually, the reset IC is implemented by using high-voltage CMOS to realize the high accurate detect voltage $V_{detR}$, meanwhile the NVL circuit uses low-voltage CMOS to perform a low-power operation. Therefore, the threshold voltage of the NVL circuit is lower than that of the reset IC, i.e., the NVL circuit starts the recall operation by the trigger of the incorrect reset signal as shown in Fig. 14 (b).

To overcome this problem, a voltage-level checker (VLC) is introduced to the NVFF controller as shown in Fig. 15 (a). The VLC is a kind of buffer circuit in which output depends on $V_{DD}$ in case of an enabling signal EN being low, as shown in Fig. 15 (b). Even if the reset signal becomes high, the output signal of VLC keeps low when $V_{DD}$

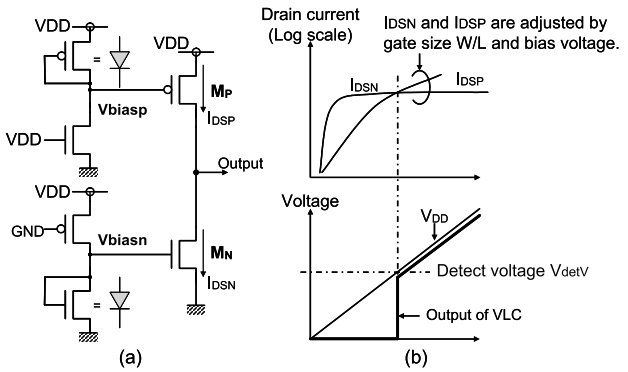



**Fig. 16** Voltage-detect circuit. (a) Simplified schematic. (b) Design of the detect voltage $V_{detV}$.

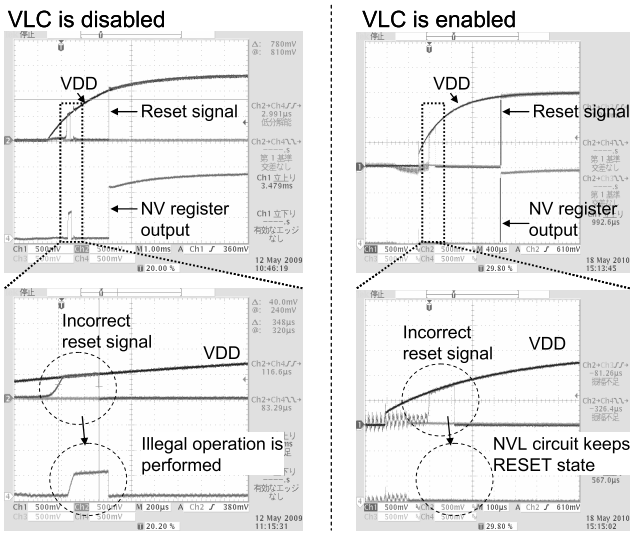



**Fig. 17** Experimental result of the VLC.

is lower than the specified detect voltage $V_{detV}$. In the proposed VLC, $V_{detV}$ is set between the threshold voltage of the reset IC and $V_{detR}$. Since accuracy of $V_{detR}$ is relatively low, the voltage-detect circuit can be implemented by a simple circuit as shown in Fig. 16 (a).

In this circuit, $V_{detV}$ is determined by drain current $I_{DSN}$ of an NMOS transistor $M_N$ and $I_{DSP}$ of a PMOS transistor $M_P$ as shown in Fig. 16 (b), where characteristics of $I_{DSN}$ and $I_{DSP}$ are controlled by $\beta$ ratio and the gate bias of $M_N$ and $M_P$. Since static current flows in the voltage-detect circuit incurs large loss of the static power, the current flow is cut off when the reset signal is low, or the output of VLC, which is used as an enabling signal EN of the VLC, becomes high.

Figure 17 shows an experimental result of the VLC. When the VLC is disabled, an output of the NVFF changes after the positive or negative edge of the incorrect reset signal, which means that the NVL circuit performs the illegal recall and store operations at $V_{DD} = 0.5$V. On the other hand, the use of VLC makes it possible to forbid any operation if $V_{DD}$ is lower than $V_{detV}$. Since $V_{detV}$ is higher than the

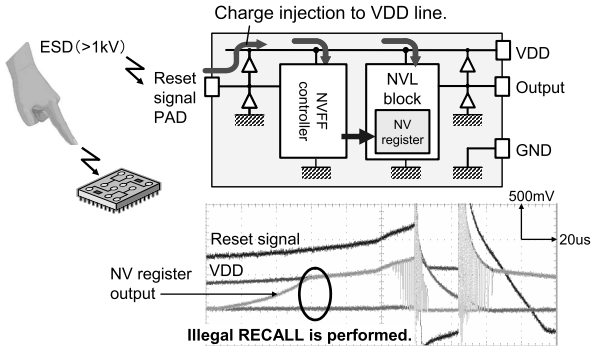



**Fig. 18** Illegal store and recall operations caused by ESD.

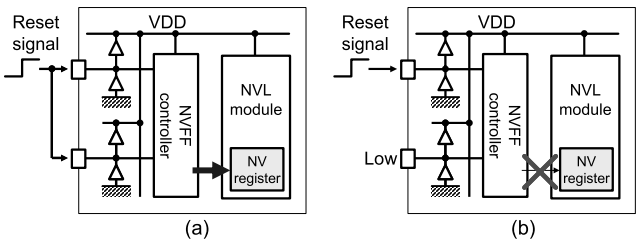



**Fig. 19** Reset signal interface using two I/O PADs. (a) Store and recall operations are enabled. (b) Store and recall operations are disabled.

threshold voltage of the reset IC, the incorrect reset noise is neglected from the NVFF controller.

### 3.2 ESD Protection

The illegal store and recall operations are sometime caused by electro-static discharge (ESD) pulses from the operating environment and peripherals. When ESD is applied to an I/O PAD of an LSI, electrical charge transfers from the I/O PAD to the $V_{DD}$ line through a protection diode, i.e., the power supply for LSI turns on [15]. Therefore, the illegal operation is possibly performed by a signal noise on a reset-signal PAD as shown in Fig. 18.

In the proposed NVL circuit, two I/O PADs are used to receive the reset signals in order to forbid the illegal operation. During ESD applied, an ESD-applied PAD goes high, but others keep low because each I/O PAD is isolated by the protection diode. Therefore, if only one PAD goes high, the LSI possibly works by the power supply of ESD. From this point of view, the proposed NVL performs store and recall operations only when the same reset signal is applied to two I/O PADs simultaneously as shown in Fig. 19 (a). Otherwise, the store and recall operations are disabled, i.e., stored data in FE capacitors are protected from the illegal access caused by ESD pulses as shown in Fig. 19 (b).

## 4. Design of NVL Circuits

### 4.1 Design Flow

The design flow of the proposed NVL circuit is same to that of the conventional one except for NV replacement. A given

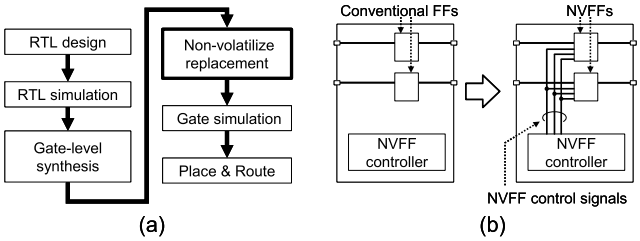



**Fig. 20** Design flow of an NVL circuit. (a) Design flow chart. (b) Non-volatile replacement.

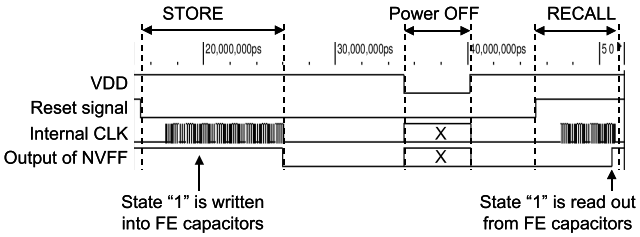



**Fig. 21** Waveforms of a gate-level simulation.

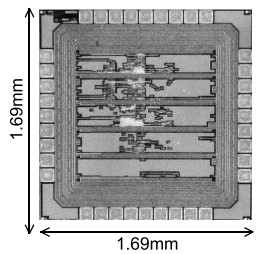



**Fig. 22** Photograph of an NV counter.

RTL specification is synthesized into a gate netlist together with the NVFF controller module as shown in Fig. 20 (a). Then, all conventional FFs in a target logic module are replaced by NVFFs. At the same time, signal wires used to transit NVFF control signals are connected to the NVFF controller and NVFFs as shown in Fig. 20 (b). Since the performance of the NVFF is the same as that of the conventional one in a logic operation, timing mismatch will not occur after the NV replacement. Figure 21 shows an example of the simulation waveform using the NVFF-based gate netlist, in which state of the NVFF becomes arbitrary during power off. A state of the NVFF is correctly recovered after the recall operation, i.e., the store and recall operations are correctly performed with the negative and positive edge of the reset signal, respectively. As shown in this example, the basic function of the designed NVL circuit is strictly verified by using proposed design environment.

### 4.2 Design Examples

The proposed NVL circuit has already been applied to some prototype chips such as a binary counter, a power-getable reconfigurable logic chip [10] and a non-volatile CPU [11].

Figure 22 shows a photograph of a 4-bit NV counter

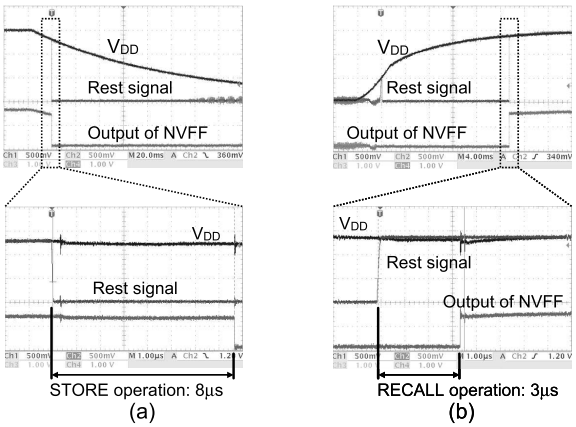



**Fig. 23** Measured waveforms. (a) Store operation. (b) Recall operation.

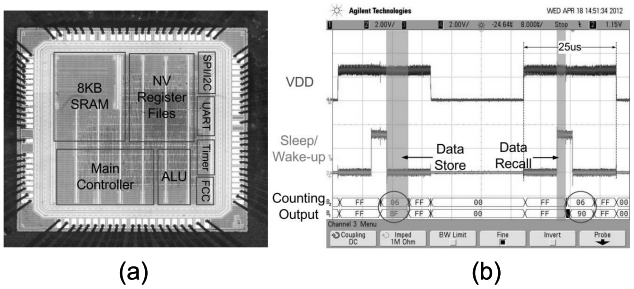



**Fig. 24** Non-volatile CPU THU1010N [11]. (a) Photograph of the prototype chip. (b) Continuously counting under 20KHz interrupted power supply.

**Table 2** Data store and recall energy consumption of three different data backup locations [11].

| Data backup location | Data store energy ($\mu J$) | Data recall energy ($\mu J$) |
|---|---|---|
| FeFF (NVFF) | 0.023 | 0.008 |
| Off-chip Flash | 2060 | 1.3 |
| On-chip Flash | 445 | 0.6 |

chip using 130nm CMOS with PZT thin film, which includes four NVFFs. The function of the NV counter is same as that of standard 4-bit counter, 74HC161 [13]. Figures 23 (a) and (b) show measured waveforms of the store and recall operations, respectively, with a reset IC of $V_{detR}$ = 1.3V. The store and recall operations are performed at delay time of 8$\mu$s at $V_{DD}$ = 1.2V and 3$\mu$s at $V_{DD}$ =1.3V, respectively, which are short enough to perform these operations during rising and falling of $V_{DD}$.

Since the write and read access for FE capacitors are performed in parallel, delay time of the store and recall operations is independent of the number of NVFFs. Figure 24 (a) shows a photograph of the NV CPU, named as THU1010N, using same process as the NV counter [11]. As shown in Fig. 24 (b), the store and recall operations for 1.6k NVFFs are performed in 7$\mu$s and 3$\mu$s at $V_{DD}$ = 1.5V, respectively, which are almost same to that of the NV counter.

Table 2 shows comparison of energy consumption

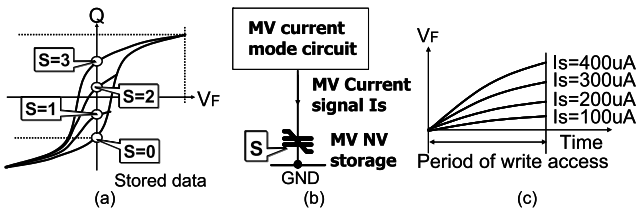



**Fig. 25** Multiple-valued data storage using an FE capacitor. (a) Minor hysteresis characteristics. (b) Write operation using current-mode logic. (c) Applied voltage across the FE capacitor.

for store and recall of 1.6k data by three different methods, THU1010N, off-chip flash memory and on-chip flash memory. Comparing THU1010N with other two methods, THU1010N can decrease the energy consumption by 19000 times in the data store and 74 times in the data recall.

## 5. Conclusion

In this paper, an FE-based non-volatile logic is proposed for low-power LSI. During standby state, the state of the NVFF is retained in FE capacitors without power supply. Standby currents in a logic circuit can be cut off, which reduces the standby power to zero. The use of complementarily stored data in coupled FE capacitors makes it possible to guarantees 10 year retention at 85 degree Celsius at 0.9-1.5V read/write operations. The low supply voltage and electrostatic discharge (ESD) detection technique prevent data destruction caused by illegal access to FE capacitors during standby state. Any logic LSI can become non-volatilized by using this technology without degradation of the performance. Applying the proposed circuitry in CPU, the write and read operations for all FE capacitors in 1.6k-bit NVFFs are performed within 7$\mu$s and 3$\mu$s with access energy of 23.1$n$J and 8.1$n$J, respectively.

The use of FE capacitor-based NVL may contribute to reduce power dissipated in not only binary CMOS logic but also in multiple-valued (MV) logic. The multiple-valued non-volatile storage is realized by using minor hysteresis characteristics of the FE capacitor as shown in Fig. 25 (a). The remnant polarization charges of each FE capacitor are determined by applied voltage $V_F$ across the FE capacitor, which corresponds to current flow $I_S$ as shown in Fig. 25 (b), (c). In case of MV current-mode logic (MVCML) [14] based circuit, an operation result is obtained by current signal $I_S$. Therefore, MV data can be stored into the FE capacitors by using $I_S$. During standby state, stored data is retained in FE capacitors, power supply for MVCML can be cut off, that is, standby power can be reduced to zero.

### References

[1] L.T. Clark, "Low standby power state storage for sub-130-nm technologies," IEEE J. Solid-State Circuits, vol.40, no.2, pp.498–506, Feb. 2005.
[2] T.-C. Chen, "Where CMOS is going: Trendy hype vs. real technology," IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, 2006, pp.22–28, 2006.

[3] Y. Shin, S. Heo, H.-O. Kim, and J.Y. Choi, "Supply switching with ground collapse: Simultaneous control of subthreshold and gate leakage current in nanometer-scale CMOS circuits," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol.15, no.7, pp.758–766, July 2007.
[4] Y. Fujimori, T. Nakamura, H. Takasu, H. Kimura, T. Hanyu, and M. Kameyama, "Ferroelectric non-volatile logic devices," Integrated Ferroelectrics, vol.56, pp.1003–1012, 2003.
[5] S. Sugibayashi, R. Nebashi, and N. Kasai, "Nonvolatile magnetic flip-flop for standby-power-free SoCs," IEEE Custom Integrated Circuits Conf., 2008, pp.14-4-1–14-4-4, 2008.
[6] ROHM, "Low voltage free delay time setting CMOS voltage detector IC series," BU42xx and BU43xx series datasheet, Feb. 2014.
[7] Y. Doyle, Y.J. Lee, Y. Kim, H. Wilsch, and F. Lombardi, "A CMOS subbandgap reference circuit with 1-V power supply voltage," IEEE J. Solid-State Circuits, vol.39, no.1, pp.252–255, 2004.
[8] A. Sheikholeslami and P.G. Gluak, "A survey of circuit innovations in ferroelectric random-access memories," Proc. IEEE, vol.88, no.5, pp.667–689, 2000.
[9] H. Kimura, T. Hanyu, M. Kameyama, Y. Fujimori, N. Nakamura, and H. Takasu, "Complementary ferroelectric-capacitor logic for low-power logic-in-memory VLSI," IEEE J. Solid-State Circuits, vol.39, no.6, pp.919–926, 2004.
[10] M. Ikeda, M. Koba, K. Inoue, M. Amagasaki, Y. Ichida, M. Saji, J. Iida, and T. Sueyoshi, "A genuine power-gatable reconfigurable logic chip with FeRAM cells," IEICE Trans. Electron., vol.E94-C, no.4, pp.548–556, April 2011.
[11] Y. Wang, Y. Liu, Y. Liu, D. Zhang, S. Li, B. Sai, M. Chiang, and H. Yang, "A compression-based area-efficient recovery architecture for nonvolatile processors," IEEE The Design, Automation, and Test in Europe (DATE) Conf., 2012.
[12] Y. Wang, Y. Liu, S. Li, D. Zhang, B. Zhao, M. Chiang, Y. Yan, B. Sai, and H. Yang, "A 3$\mu$s wake-up time nonvolatile processor based on ferroelectric flip-flops," European Solid-State Circuits Conf. (ESSCIRC), 2012.
[13] TOSHIBA, "CMOS digital integrated circuit silicon monolithic," TC74HC161 datasheet, May 2001.
[14] H. Shirahama, T. Matsuura, M. Natsui, and T. Hanyu, "Energy-aware multiple-valued current-mode sequential circuit using a completion-detection scheme," IEICE Trans. Inf. & Syst., vol.E93-D, no.8, pp.2080–2088, Aug. 2010.
[15] J.M. Rabaey, A. Chandrakasan, and B. Nikolic, Digital Integrated Circuit, 2nd ed., Pearson Education, USA, 2003.

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